5G SRM815 Module Hardware Design Manual

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Add：32/F,Building B,Shenzhen International Innovation Center, No.1006 Shennan Avenue,Futian District,Shenzhen,China
Tel：+86-755-83218588 Fax：+86-755-83219788
E-mail：ir@meigsmart.com Web：www.meigsmart.com

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Revision History

No.	Version Number	Date	Author	Reason for Revision
1	V1.0	3/5/2020	Yang Shuang	Establish for the first version
2	V1.1	6/28/2020	Yang Shuang	Modify antenna port mapping Add reserved pin 198PIN for RF signal control Add reserved pin 281PIN, can be used for SLIC_INT control signal

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1 Introduction

This document defines 5G SRM815 module and the air interface and hardware interface for connecting the module to applications of customers.

This document can help customers quickly understand the interface specifications, electrical characteristics, mechanical specifications and related product information of 5G SRM815 module. With the help of this document, according to our application manual and user guide, customers can quickly apply 5G SRM815 module to wireless applications.

5G SRM815 wireless module is a type of wireless broadband terminal product suitable for various network standards such as 5G NR, LTE-TDD, LTE-FDD and WCDMA .

5G SRM815 can support the following access rates:

- 5G NR Sub-6GHz:
  -MIMO 4*4,256QAM
  -Downlink up to 4Gbps
  -Uplink up to 300Mbps
- LTE Cat 20:
  -MIMO 4*4,256QAM
  -Downlink up to 2Gbps
  -Uplink up to 200Mbps
- DC HSPA+:
  -Downlink up to 42Mbps
  -Uplink up to 5.76Mbps

Products can be widely used in CPE residential gateways, high-definition televisions, AR/VR, industrial routers, set-top boxes, on-vehicle terminals, video surveillance, industrial Internet and other fields.

1.1 Safety Instructions

By complying with the following safety principles, you can ensure personal safety and protect the products and working environment from potential damage:

	Driving safety first! When you drive, do not use handheld mobile terminal device unless it has a hands-free function. Please stop the car before calling!
	Please turn off the mobile terminal device before boarding. The wireless function of mobile terminal shall not be turned on in the aircraft to prevent interference with the aircraft communication system. Ignoring this reminder may affect flying safety or even violate the law.
	In hospitals or health care facilities, pay attention to whether there are restrictions on the use of mobile terminal device. RF interference will cause medical equipment to be abnormal, so mobile terminal device may need to be turned off.
	Mobile terminal device cannot always be effectively connected, for example, if the mobile device has no expense or the SIM is invalid. When you encounter the above situations in an emergency, please make an emergency call, meanwhile, ensure that your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and transmit radio frequency signals when it is turned on. There will be radio frequency interference when it is close to TV, radio, computer or other electronic equipment.
	Please keep mobile device away from inflammable gases. Please turn off the mobile terminal device when you are near a fueling station, oil depot, chemical plant or explosion site. There will be potential safety hazards when operating electronic equipment in any place with potential explosion hazard.

1.2 Purpose of the Document

This document details the basic functions, main features, hardware interfaces and usage, structural characteristics, power consumption indexes and electrical characteristics of 5G SRM815 wireless module, and guides users to embed 5G SRM815 module in various application terminals.

1.3 List of Contents

This document is divided into the following parts:

- Chapter 1 mainly describes safety instructions, purpose of the document and overview of contents, etc .;
- Chapter 2 describes the basic functions and main features of 5G SRM815 wireless module;
- Chapter 3 describes in detail the functions, features and usage of each hardware interface of 5G SRM815;
- Chapter 4, related characteristics of GNSS;
- Chapter 5, related contents and precautions of antenna interface;
- Chapter 6 describes in detail the electrical characteristics of 5G SRM815;
- Chapter 7 describes in detail the structural characteristics and precautions of 5G SRM815;
- Chapter 8 describes in detail the storage and production considerations of 5G SRM815;
- Chapter 9, Annex A Reference Documents and Abbreviations;
- Chapter 10, Annex B GPRS Coding Scheme.

2 Product Overview

2.1 Basic Description

5G SRM815 is a type of wireless communication module supporting 5G NR , LTE-TDD, LTE-FDD and WCDMA. It supports 5G NR, TDD-LTE and FDD-LTE network data connection, and it is downward compatible with DC-HSPA+ network data connection of WCDMA. It can provide voice (PCM), analog voice, short message, address book and other functions for special applications of customers.

5G SRM815 module has 2 sub-models: 5G SRM815-EA and 5G SRM815-NA. The following table lists the frequency bands supported by these 2 sub-models:

Table 1 Frequency Bands Supported by 5G SRM815 Module

The Internet	5G SRM815-EA	5G SRM815-NA
5G NR	N1/N3/N5/N7/N8/N20/N28/N38/N40/N41/N77/N78/N79	N2/N5/N12/N25/N41/N48/N66/N71/N78
TDD-LTE	B34/B38/B39/B40/B41/B42	B41/B42/B43/B48
FDD-LTE	B1/B3/B5/B7/B8/B18/B19/B20/B28/B32	B2/B4/B5/B12/B13/B14/B25/B26/B28/B29/B30/B66/B71
WCDMA	B1/B3/B5/B8	B2/B4/B5

5G SRM815 adopts an advanced and highly integrated design scheme, integrating RF and baseband on a PCB to complete the functions of wireless receiving, transmission, baseband signal processing and audio signal processing. With single-sided layout, the structural size of the module is 44mm*41mm*2.8mm. It can meet almost all M2M application requirements, for example, it can be used for mobile broadband access, video surveillance, handheld terminals, on-vehicle equipment, ultrabooks and other products.

2.2 Main Performance

The following table details the performance of 5G SRM815module.

Table 2 Main Features of the Module

Parameter	Notes
Power supply	● VBAT supply voltage range: 3.3V～4.3V ● Typical supply voltage: 3.8V
Transmitting power	● Class 2 (26dBm+2/-3dB) for 5G NR HPUE ● Class 3 (23dBm±2.7dB) for TDD-LTE bands ● Class 3 (23dBm±2.7dB) for FDD-LTE bands ● Class 3 (24dBm+1.7/-3.7 dB) for WCDMA bands
5G NR features	● Support 3GPP R15 standard ● Support SA/NSA
LTE features	● Support up to 7CA CAT20 ● Support radio frequency bandwidth of 1.4 ~ 20MHz ● Support multi-user MIMO in downlink ● Max. uplink rate 200Mbps, Max. downlink rate 2 Gbps
WCDMA features	● Support 3GPP R8 DC-HSPA+ ● Support 16-QAM, 64-QAM and QPSK modulation ● 3GPP R6 CAT6 HSUPA: Max. uplink rate 5.76Mbps ● 3GPP R8 CAT24 DC-HSPA+: Max. downlink rate 42Mbps
Network protocol features	● Support TCP/UDP/PPP/ PING/NITZ/QMI protocol ● Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol)
Short Message Service (SMS)	● Text and PDU modes ● Point-to-point MO and MT ● Short message storage: stored in the module by default
USIM card interface	● Support USIM/SIM card: 1.8V and 3V
Audio features	● Support 2 digital audio interfaces: PCM interface and I2S interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● 5G NR: AMR/AMR-WB
PCM interface	● For audio use, external codec chip is required ● Support 8-bit A-law, u-law and 16-bit linear coding formats ● Support long frame mode and short frame mode ● Support master and slave modes, but it can only be used as master mode in long frames
USB interface	● Compatible with USB3.1 gen2 feature (only supporting slave mode), max. data transmission rate 10.0Gbps ● Used for AT command, data transmission, GNSS NMEA output, software debugging and upgrade ● USB driver: Support Windows7, Windows 8/8.1, Windows10, Linux 2.6 or higher versions, Android2.3/4.0/4.2/4.4/5.0/5.1/6.0/7.0/8.0/9.0/10.0

Serial port	Main serial port: ● Used for AT command and data transmission ● The maximum baud rate is 460800bps, and the default is 115200bps ● Support RTS and CTS hardware flow control Debug serial port: ● Used for Linux control, log output ● The baud rate is 115200bps
Wireless connection interface	● Support low power UART Bluetooth interface
RGMII interface	● Support 10/100/1000Mbps Ethernet connection
SD card interface	● Compliant with SD3.0protocol
GNSS features	● Qualcomm Gen8C-Lite ● Protocol: NMEA 0183
RX-diversity	● Support 5G NR/LTE/WCDMA diversity
AT command	● Compliant with 3GPP TS 27.007 and 27.005, newly add MeiG AT command
Network indication	● NET_STATUS and NET_MODE these two pins indicate network status
Antenna interface	● 5G antenna interface ANT_5G_TRX0 ANT_5G_TRX1 ANT_5G_DIV0, ANT_5G_DIV1 ● 4G antenna interface ANT_4G_TRX, ANT_4G_DIV ● MIMO antenna interface ANT_PRX_MIMO, ANT_DRX_MIMO ● GNSS antenna interface ANT_GNSS
Physical properties	● Size: 44mm*41mm*2.8mm ● Weight: <10g
Temperature range	● Normal working temperature: -30℃～+75℃ ● Extended working temperature: -40℃～+85℃ ● Storage temperature: -45℃～+90℃
Software upgrade	● USB interface
RoHS	● All parts are fully compliant with EU RoHS standard
Ambient humidity	● 5%~95%
ESD (backplane testing is required)	● VBAT, GND: air discharge ±10KV, contact discharge ±5KV ● Other interfaces: air discharge ±1KV, contact discharge ±0.5KV
Interface	● LGA 392-Pin interface
LGA functional interface	● Power interface ● USB2.0 High-Speed interface/SS USB3.1 Gen2 interface ● UART interface ● USIM/SIM card interface (support 3V and 1.8V) ● PCM interface ● Hardware reset interface ● Indicator interface ● Sleep control interface ● Flight mode control interface ● ADC interface ● I2C interface ● I2S interface ● RGMII interface

- SD card interface
- PCIe interface
- BT_UART interface
- USB_BOOT interface

2.3 Functional Block Diagram

The following is a block diagram of 5G SRM815, which elaborates its main functional parts.

- Power management
- Baseband chip
- DDR+NAND memory
- RF part
- Peripheral interface

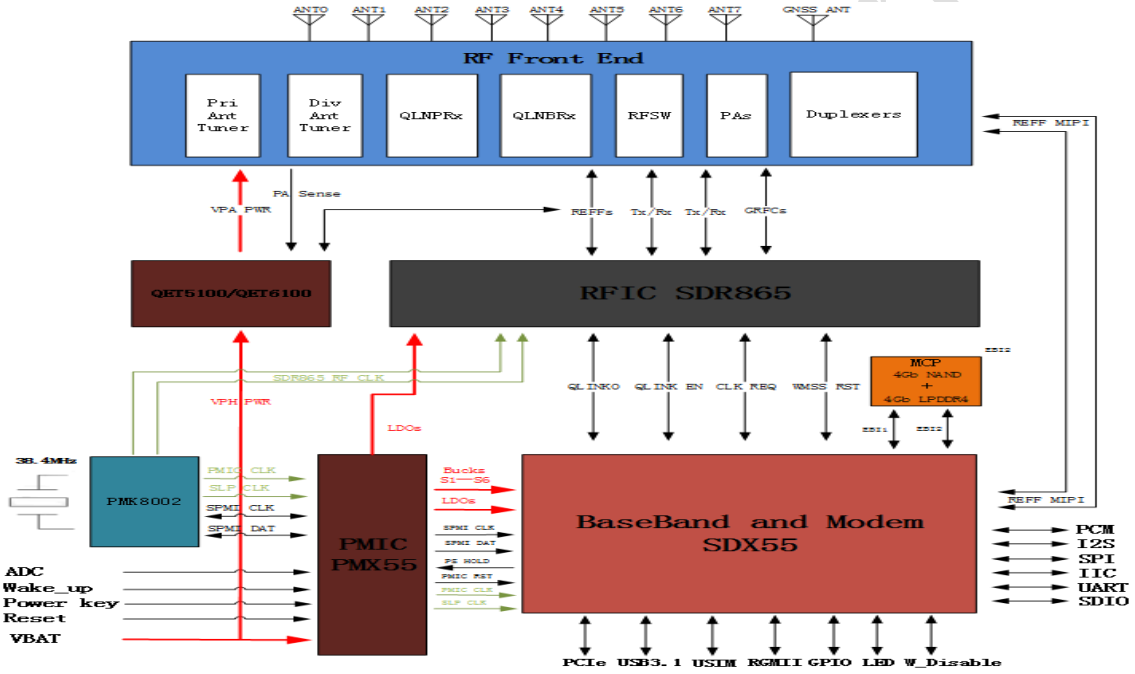

Figure 1 Functional Block Diagram

2.4 Evaluation Board

To help test and use 5G SRM815 module, MeiG Smart Technology Co., Ltd provides a set of evaluation board. Evaluation board tools include USB data cable, antenna and other peripherals.

For details on how to use the evaluation board, please refer to the 5G_EVB User Manual.

3 Application Interface

3.1 Basic Description

5G SRM815 adopts LGA interface with a total of 392 Pins and provides the following functional interfaces:

- Power interface
- USIM/SIM interface
- USB interface
- UART interface
- PCM interface
- I2C interface
- I2S interface
- SPI interface
- PCIe interface
- Hardware reset interface
- Status indication interface
- Sleep control interface
- Flight mode control interface
- ADC interface
- RGMII interface
- SD card interface
- BT_UART interface
- USB_BOOT interface

3.2 Definition of LGA Card Pin

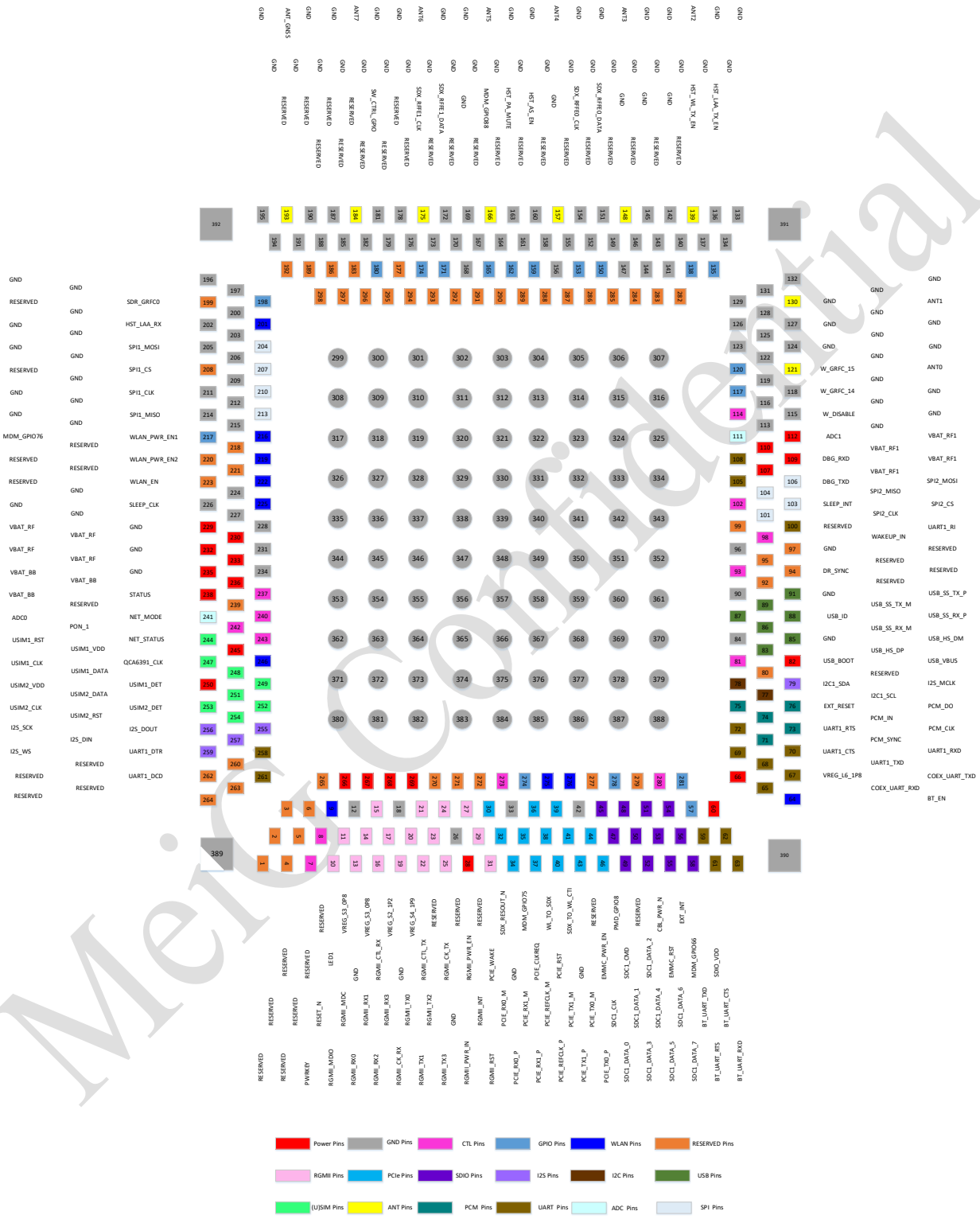

Figure 2 Serial Number of Module Pins

3.3 Pin Description

The following table shows the definition of each pin of 5G SRM815 module.

Table 3 IO Parameter Definition

Type	Description
AI	Analog input signal
AO	Analog output signal
DI	Input signal
DO	Output signal
IO	Input and output two-way signal
OD	Open-drain output signal
PI	Power input
PO	Power output

Table 4 Pin Description

Power Supply					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
VBAT_BB	235, 236, 238	PI	Module baseband power supply	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide the current up to 1A.
VBAT_RF	229, 230, 232, 233	PI	Module RF Power supply	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide the current up to 2A.
VBAT_RF1	107, 109, 110, 112	PI	Module RF Power supply	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide the current up to 2A.
VREG_L6_1P8	66	PO	Module output 1.8V	Vnorm=1.8V $I_o$max50mA	It can provide pull-up for external GPIO
GND	12, 18, 26, 33, 42, 84, 90, 96, 113, 115, 116, 118, 119, 122-129, 131-134,	-	Ground	-	-

	136, 137, 140-147, 149, 151, 152, 154-156, 158, 160, 161, 163, 164, 167-170, 172, 173, 176-179, 181, 182, 185, 187, 188, 190, 191, 194-197, 200, 202, 203, 205, 206, 209, 211, 212, 214, 215, 224, 226-228, 231, 234, 299-392				
Start/Shut Down					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
RESET_N	8	DI	Reset module		1.8V power domain, active low, not connected when not in use.
PWRKEY	7	DI	Module starting/shutdown		1.8V power domain, pulse switch
PON_1	242	DI	Long pull-up to start the module		Pull down 10K resistor to ground by default
CBL_PWR_N	280	DI	Long pull-down to start the module		NC when not in use
Module Status Indication					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
STATUS	237	OD	Indicate the running status of the module		External pull-up is required, with the sink current capability up to

					10mA
NET_MODE	240	DO	Indicate the network registry status of the module		1.8V power domain, NC when not in use
NET_STATUS	243	DO	Indicate the network operation status of the module		1.8V power domain, when not in use, it shall be grounded through 10K resistor
USB Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
USB_VBUS	82	PI	USB detection	Typical voltage 5V	
USB_HS_DP	83	IO	USB differential data positive signal	Compliant with USB2.0 specifications	
USB_HS_DM	85	IO	USB differential data negative signal	Compliant with USB2.0 specifications	
USB_SS_TX_P	91	AO	USB transmits positive signal at high speed	Compliant with USB3.1 Gen2 specifications	90Ω differential impedance is required
USB_SS_TX_M	89	AO	USB transmits negative signal at high speed		
USB_SS_RX_P	88	AI	USB receives positive signal at high speed		
USB_SS_RX_M	86	AI	USB receives negative signal at high speed		
USIM Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
USIM1_VDD	245	PO	USIM1 card power supply	**1.8V USIM:** Vmax=1.9V Vmin=1.7V **3.0V USIM:** Vmax=3.05V Vmin=2.75V $I_O$max=50mA	The module automatically identifies 1.8V or 3.0V USIM card
USIM1_DATA	248	IO	USIM1 card data signal		It needs to connect pull-up to USIM1_VDD
USIM1_CLK	247	DO	USIM1 card clock signal		

USIM1_RST	244	DO	USIM1 card reset signal		
USIM1_DET	249	DI	USIM1 card detection signal		1.8V power domain, it needs external pull-up to 1.8V; if hot plug is not required, this signal is NC
USIM2_VDD	250	PO	USIM2 card supply voltage	**1.8V USIM:** Vmax=1.9V Vmin=1.7V **3.0V USIM:** Vmax=3.05V Vmin=2.7V $I_o$max=50mA	The module automatically identifies 1.8V or 3.0V USIM card. If USIM2 is not used, it is recommended to connect this pin to VREG_L6_1P8 (66Pin)
USIM2_DATA	251	IO	USIM2 card data signal		It needs to connect pull-up to USIM2_VDD, not connected when not in use.
USIM2_CLK	253	DO	USIM2 card clock signal		
USIM2_RST	254	DO	USIM2 card reset signal		
USIM2_DET	252	DI	USIM2 card detection signal		1.8V power domain, it needs external pull-up to 1.8V; if hot plug is not required, this signal is NC
Main Serial Port Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
UART1_RI	100	DI	Ringing reminder		1.8V power domain, not connected when not in use.
UART1_DCD	261	DI	Used for data connection Status detection		1.8V power domain, not connected when not in use.
UART1_DTR	258	DO	Data terminal ready		1.8V power domain, not connected when not in use.
UART1_RXD	70	DI	Module receives data		1.8V power domain, not connected when not in use.
UART1_TXD	68	DO	Module transmits data		1.8V power domain, not connected when

					not in use.
UART1_CTS	69	DO	Clear to send		1.8V power domain, not connected when not in use.
UART1_RTS	72	DI	Request to send		1.8V power domain, not connected when not in use.
Bluetooth Serial Port Interface					
BT_UART_TXD	59	DO	Transmit data		1.8V power domain, not connected when not in use.
BT_UART_RXD	63	DI	Receive data		1.8V power domain, not connected when not in use.
BT_UART_RTS	61	DI	Request to send		1.8V power domain, not connected when not in use.
BT_UART_CTS	62	DO	Clear to send		1.8V power domain, not connected when not in use.
ADC Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
ADC0	241	AI	General-purpose analog-to-digital conversion	Voltage range: 0 V~1.875V	Not connected when not in use.
ADC1	111	AI	General-purpose analog-to-digital conversion	Voltage range: 0 V~1.875V	Not connected when not in use.
Debug Serial Port					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
DBG_TXD	105	DO	Module transmits data		1.8V power domain, not connected when not in use.
DBG_RXD	108	DI	Module receives data		1.8V power domain, not connected when not in use.
USB_BOOT interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
USB_BOOT	81	DI	Forced download mode control		Connect to 1.8V to enter forced loading mode, it is recommended to

				reserve test points
I2C interface				
I2C1_SCL	77	OD	I2C clock signal	1.8V power domain, external 1.8V pull-up is required, not connected when not in use.
I2C1_SDA	78	OD	I2C data signal	1.8V power domain, external 1.8V pull-up is required, not connected when not in use.
I2S Interface				
I2S_MCLK	79	IO	I2S master clock	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
I2S_WS	259	IO	I2S synchronous clock signal	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
I2S_SCK	256	IO	I2S bit clock	1.8V power domain, if the module is used as the master unit, this pin is an

					output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
I2S_DIN		257	DI	I2S input signal	1.8V power domain, not connected when not in use.
I2S_DOUT		255	DO	I2S output signal	1.8V power domain, not connected when not in use.
PCM Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
PCM_SYNC		71	IO	PCM data synchronization signal	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
PCM_CLK		73	IO	PCM clock	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
PCM_IN		74	DI	PCM data input signal	1.8V power domain, not connected when not in use.
PCM_OUT		76	DO	PCM data output signal	1.8V power domain, not connected when not in use.
SPI Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
SPI1_CLK		210	DO	SPI clock signal	1.8V power domain, only support master

					mode
SPI1_CS	207	DO	SPI chip select		1.8V power domain, only support master mode
SPI1_MISO	213	DI	SPI master input slave output		1.8V power domain, only support master mode
SPI1_MOSI	204	DO	SPI master output slave input		1.8V power domain, only support master mode
RF interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
ANT0	121	IO	LMHB TRX n41 TRX1 n79_DRX1	50Ω characteristic impedance	Not connected when not in use
ANT1	130	IO	LMHB DRX n41_DRX1 n79_TRX1		
ANT2	139	AI	n79_DRX0		
ANT3	148	IO	n79_TRX0		
ANT4	157	IO	MHB PRX_MIMO n77/78 TRX0 UHB TRX		
ANT5	166	IO	n77/78 TRX1 n41 TRX0 UHB TRX1		
ANT6	175	AI	MHB DRX_MIMO n77/78 DRX0 n41 DRX0 UHB DRX		
ANT7	184	AI	n77/78 DRX1 UHB DRX1		
ANT_GNSS	193	AI	GNSS antenna		
WLAN Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
WLAN_PWR_EN2	219	DO	WLAN power enable signal		1.8V power domain, active high, not connected when not in use.
WLAN_PWR_EN1	216	DO	WLAN power enable signal		1.8V power domain, active high, not connected when not in use.

WLAN_EN	222	DO	WLAN enabled, active high	1.8V power domain, active high, not connected when not in use.
COEX_UART_RXD	65	DI	WSI interface adopts WLAN/WAN Coex algorithm	1.8V power domain, not connected when not in use.
COEX_UART_TXD	67	DO	WSI interface adopts WLAN/WAN Coex algorithm	1.8V power domain, not connected when not in use.
SLEEP_CLK	225	DO	Sleep clock output	Not connected when not in use
HST_LAA_RX	201	DO	Module controls WLAN 5G LNA to enter isolation mode signal	1.8V power domain, not connected when not in use.
HST_AS_EN	159	DO	n79 / LAA turns off WLAN 5G signal	1.8V power domain, not connected when not in use.
HST_PA_MUTE	162	DO	SDX controls to turn off WLAN PA signal	1.8V power domain, not connected when not in use.
HST_LAA_TX_EN	135	DO	n79 / LAA controls WLAN 5G PA to enter isolation mode signal	1.8V power domain, not connected when not in use.
HST_WL_TX_EN	138	DO	WLAN controls N79/LAA signal and turns off the corresponding LNA	1.8V power domain, not connected when not in use.
SDX_TO_WL_CTI	276	DO	Module controls WLAN signal	1.8V power domain, not connected when not in use.
SW_CTRL_GPIO	180	DI	Switching control signal	1.8V power domain, not connected when not in use.
WL_TO_SDX	275	DO	WLAN wakes up module signal	1.8V power domain, not connected when not in use.
VREG_S4_1P9	269	PO	1.9V power output	Provide power supply for QCA6391 WiFi IC when it is adapted, NC when

					not in use
VREG_S2_1P2	268	PO	1.2V power output		Provide power supply for QCA6391 WiFi IC when it is adapted, NC when not in use
VREG_S3_0P8	266, 267	PO	0.8V power output		Provide power supply for QCA6391 WiFi IC when it is adapted, NC when not in use
RGMII Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
RGMII_MDIO	10	IO	MDIO interface data input/output signal		1.8V power domain, not connected when not in use.
RGMII_MDC	11	DO	RGMII interface clock output		1.8V power domain, not connected when not in use.
RGMII_RX0	13	DI	RGMII interface receives data bit0		50Ω impedance control, 1.8V power domain, not connected when not in use.
RGMII_RX1	14	DI	RGMII interface receives data bit1		
RGMII_CTL_RX	15	DI	RGMII interface receives control signal		
RGMII_RX2	16	DI	RGMII interface receives data bit2		
RGMII_RX3	17	DI	RGMII interface receives data bit3		
RGMII_CK_RX	19	DI	RGMII receives clock signal		

RGMII_TX0	20	DO	RGMII interface transmits data bit0	
RGMII_CTL_TX	21	DO	RGMII interface transmits data control signal	
RGMII_TX1	22	DO	RGMII interface transmits data bit1	
RGMII_TX2	23	DO	RGMII interface transmits data bit2	
RGMII_CK_TX	24	DO	RGMII interface transmits clock signal	
RGMII_TX3	25	DO	RGMII interface transmits data bit3	
RGMII_PWR_EN	27	DO	RGMII power enable control signal	1.8V power domain, not connected when not in use.
RGMII_INT	29	DI	RGMII interrupt signal	1.8V power domain, not connected when not in use.
RGMII_RST	31	DO	RGMII reset signal	1.8V power domain, not connected when not in use.
RGMII_PWR_IN	28	PI	Use an external LDO to provide 1.8V power supply for RGMII_PWR_IN	When the module supports RGMII function, 1.8V power input externally provided is required. When RGMII function is not required, this pin shall be connected to VREG_L6_1P8(66 Pin)

SDIO Interface

Pin Name	Pin Number	I/O	Description	DC Features	Remarks
SDIO_VDD	60	PI	SDIO power supply		According to SD requirements, select input voltage

					of 1.8V or 2.85V. When not in use, this pin shall be connected to VREG_L6_1P8(66 Pin)
SDC1_DATA_0	49	IO	SDC data bit0		Not connected when not in use
SDC1_DATA_1	50	IO	SDC data bit1		Not connected when not in use
SDC1_DATA_2	51	IO	SDC data bit2		Not connected when not in use
SDC1_DATA_3	52	IO	SDC data bit3		Not connected when not in use
SDC1_CMD	48	IO	SDC control signal		Not connected when not in use
SDC1_CLK	47	DO	SDC clock signal		Not connected when not in use
SDC1_DATA_4	53	IO	SDC data bit4		1.8V power domain, not connected when not in use.
SDC1_DATA_5	55	IO	SDC data bit5		1.8V power domain, not connected when not in use.
SDC1_DATA_6	56	IO	SDC data bit6		1.8V power domain, not connected when not in use.
SDC1_DATA_7	58	IO	SDC data bit7		1.8V power domain, not connected when not in use.
EMMC_RST	54	DO	EMMC reset signal		1.8V power domain, not connected when not in use.
EMMC_PWR_EN	45	DO	EMMC power enable signal		1.8V power domain, not connected when not in use.
PCIe Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
PCIE_REFCLK_P	40	AO	PCIe differential clock positive signal	Compliant with PCIe Gen3.0 protocol standard	Differential 85Ω impedance control
PCIE_REFCLK_M	38	AO	PCIe differential clock negative signal		
PCIE_TX0_M	44	AO	PCIe transmits negative signal		

			differentially	
PCIE_TX0_P	46	AO	PCIe transmits positive signal differentially	
PCIE_RX0_M	32	AI	PCIe receives negative signal differentially	
PCIE_RX0_P	34	AI	PCIe receives positive signal differentially	
PCIE_TX1_M	41	AO	PCIe transmits negative signal differentially	
PCIE_TX1_P	43	AO	PCIe transmits positive signal differentially	
PCIE_RX1_M	35	AI	PCIe receives negative signal differentially	
PCIE_RX1_P	37	AI	PCIe receives positive signal differentially	
PCIE_CLKREQ	36	IO	PCIe data request signal	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
PCIE_RST	39	IO	PCIe reset signal	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module is used as a slave, this pin is an input signal. Not connected when not in use.
PCIE_WAKE	30	IO	PCIe wake-up signal	1.8V power domain, if the module is used as the master unit, this pin is an output signal; if the module

				is used as a slave, this pin is an input signal. Not connected when not in use.
Other Interfaces				
BT_EN	64	DO	Bluetooth enable signal	1.8V power domain
EXT_RESET	75	DO	SLIC reset signal	
EXT_INT	281	DI	SLIC interrupt signal	
DR_SYNC	93	DO	1PPS clock synchronization output signal	
WAKEUP_IN	98	DI	Sleep mode control signal	
SLEEP_IND	102	DO	Module status indication	
W_DISABLE	114	DI	Flight mode control	
USB_ID	87	IO	Ordinary GPIO that can only be used as input and output judgments	
SPI2_CS	203	IO	It can be used as common GPIO	
SPI2_CLK	101	IO	It can be used as common GPIO	
SPI2_MOSI	106	IO	It can be used as common GPIO	
SPI2_MISO	104	IO	It can be used as common GPIO	
SDX_RESOUT_N	273	DO	Reset output signal	
MDM_GPIO88	165	IO	Reserved GPIO	
MDM_GPIO75	274	IO	Reserved GPIO	
MDM_GPIO76	217	IO	Reserved GPIO	
QCA6391_CLK	246	AO	38.4MHz clock output	
LED1	9	OD	Indicator light, with sink current capability	External pull-up is required, with the sink current capability up to 10mA

PMD_GPIO8	278	OD	Reserved GPIO		
SDX_RFFE0_CLK	153		RF MIPI signal		
SDX_RFFE0_DATA	150		RF MIPI signal		
SDX_RFFE1_CLK	174		RF MIPI signal		
SDX_RFFE1_DATA	171		RF MIPI signal		
W_GRFC_14	117	DO	RF control signal		
W_GRFC_15	120	DO	RF control signal		
SDR_GRFC0	198	DO	RF control signal		
Reserved interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Features**	**Remarks**
RESERVED	1, 2, 3, 4, 5, 6, 80, 92, 94, 95,97,99,177, 183,186, 189, 192,198, 199, 208,218, 220, 221,223,239, 260,262,263, 264, 265,270, 271,272,277, 279, 282-298		Reserve		Keep unconnected

Remarks: 1. * means that the function is being developed;

3.4 Working Modes of the Module

Table 5 Working Modes

Modes	Description	
WCDMA mode	WCDMA IDLE	The module system is in an idle state, the module has been registered in WCDMA network, and the module is ready to receive and transmit.
	WCDMA TALK	The module is in WCDMA voice service, the power consumption of the module depends on the network settings.
	WCDMA DATA	The module is in WCDMA data transmission,the power consumption of the module depends on the network settings (such as the power control level), data uplink and downlink rates, and related settings of WCDMA.

HSPA mode	HSPA IDLE	The module is ready for HSPA data transmission. However, there is no data receiving or transmission at this time. The power consumption of the module depends on the network settings.
	HSPA DATA	The module is in HSPA data transmission,the power consumption of the module depends on the network settings (such as the power control level), data uplink and downlink rates, and related settings of HSPA.
FDD-LTE mode	FDD-LTE IDLE	The module is ready for FDD-LTE data transmission. However, there is no data receiving or transmission at this time. The power consumption of the module depends on the network settings.
	FDD-LTE DATA	The module is in FDD-LTE data transmission, the power consumption of the module depends on the network settings (such as the power control level), data uplink and downlink rates, and related settings of FDD-LTE.
TDD-LTE mode	TDD-LTE IDLE	The module is ready for TDD-LTE data transmission. However, there is no data receiving or transmission at this time. The power consumption of the module depends on the network settings.
	TDD-LTE DATA	The module is in TDD-LTE data transmission, the power consumption of the module depends on the network settings (such as the power control level), data uplink and downlink rates, and related settings of TDD-LTE.
5G NR mode	NR IDLE	The module is ready for NR data transmission. However, there is no data receiving or transmission at this time. The power consumption of the module depends on the network settings.
	NR DATA	The module is in NR data transmission, the power consumption of the module depends on the network settings (such as the power control level), data uplink and downlink rates, and related settings of NR.
Minimum function mode		VBAT continuously supplies power. Use AT+CFUN=0 to make the module enter the minimum function mode. At this time, RF transceiver unit of the module is turned off. Use AT+CFUN=1, the module restarts the transceiver registration network to normal function mode.
Flight mode		W_DISABLE pin can set the module to flight mode. In this mode, RF does not work.
Sleep mode		In this mode, the power consumption of the module will be reduced to very low, but the module can still receive paging, short message, phone call and TCP/UDP data.
Shutdown mode		VBAT is shut down at low voltage. In this mode, PMU stops power supply for baseband (BB) and radio frequency (RF), the software stops working and the serial port fails.

3.5 Energy Saving Function

3.5.1 Sleep Mode

In sleep mode, 5G SRM815 can reduce power consumption to the lowest level. The following sections will detail the sleep mode of 5G SRM815.

3.5.1.1 USB Application 1

If the host supports USB suspend/resume function, the following conditions must all be met to enable the module to enter the sleep mode or exit the sleep mode:

1) Use the AT+SLEEPEN=1 command to enable the sleep function;
2) Keep WAKEUP_IN at high level;
3) The USB bus connecting the host to the module enters suspend state;
4) The host transmits resume to the module via USB and it will wake up the module.

Through the first three steps above, USB bus of the module will be suspended and then the module executes the sleep process to enter the sleep state smoothly. After the module enters the sleep state, the overall current will drop below 5mA, USB data service will be disconnected, the serial port and console will not be able to communicate.

When the module is required to work for the host to process services or for other requirements, execute step 4 above. After receiving the resume command, USB bus of the module will execute the wake-up process according to USB standard protocol, meanwhile keep the system awake.

The reference circuit is as below:

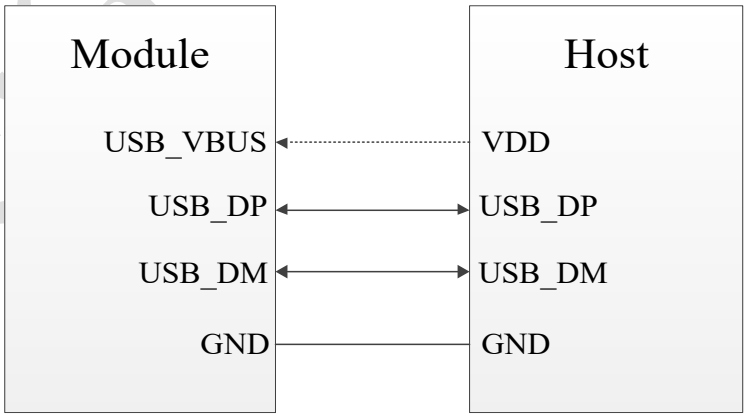

Figure 3 Sleep Application with USB Wake On LAN Function

3.5.1.2 USB Application 2

If the host does not support USB suspend function, enable the module to enter the sleep mode by

disconnecting USB bus through external control (i.e., disconnecting USB_VBUS, USB_DP and USB_DM):

1) Use the AT+SLEEPEN=1 command to enable the sleep function;
2) Keep WAKEUP_IN at high level or unconnected;
3) Disconnect USB_VBUS, USB_DP and USB_DM or remove the USB cable;
4) Restore the function of USB bus to wake up the module.

Through the first 3 steps above, the module enters the sleep mode. However, be sure to note that the module requires external power supply if entering the sleep mode in this way. Do not use USB power supply, otherwise the module will also be powered off if USB is disconnected.

After the module enters the sleep mode, when the module is required to enter normal mode to work again, execute step 4 to restore the function of USB bus, so that the module is woken up.

3.5.1.3 Hardware I/O Controls Sleep Mode

WAKEUP_IN(Pin98) pin is the pin for the module to trigger sleep. When the sleep function of the module is enabled, pull down this pin (initially at high level), the module will trigger the sleep process after detecting that the pin has a falling edge. When the sleep lock is fully released, the module will enter the sleep state smoothly.

Whether the sleep function of the module is enabled, you can use the AT command at+sleepen? to query. When the query result is 0, it indicates that the sleep function is disabled; when the result is 1, it indicates that the sleep function is enabled. Similarly, you can use the AT command at+sleepen=1 or at+sleepen=0 to enable or disable the sleep function of the module. When the sleep function of the module is disabled, all pins and states related to module sleep will be invalid, and when the USB bus is suspended, USB PHY will not enter low power mode (LPM).

When the module is in the sleep state (WAKEUP_IN pin is pulled down to trigger module sleep), pull up this pin and WAKEUP_IN will generate a rising edge. The module will trigger the wake-up after detecting that the rising edge is interrupted, then WAKEUP_IN keeps at high level and the module keeps the wake-up state.

Module control signal level supports 1.8V logic level.

3.5.2 Flight Mode

When the module enters flight mode, the radio frequency function is disabled and all AT commands related to radio frequency are not accessible. The module can enter the flight mode through hardware interface and command control.

3.5.2.1 Hardware I/O Interface Controls Flight Mode

A low level signal is sent to the module through the W_DISABLE pin (Pin 114) of 5G SRM815, and the module enters the flight mode. At this time, RF transceiver unit will stop working. Pull up Pin114, the module will re-enter the normal mode.

Module control signal level supports 1.8V logic level.

3.5.2.2 AT Command Controls Flight Mode

Send AT+CFUN=4, the module will enter the flight mode. At this time, RF transceiver unit will stop working. Send AT+CFUN=1, the module will re-enter the normal mode.

3.6 Power Supply Design

3.6.1 Pin Description

5G SRM815 has 11 VBAT pins for connecting external power supply, which can be divided into three power domains:

- Four VBAT_RF pins are used to supply power to RF of the module;
- Four VBAT_RF1 pins are used to supply power to RF of the module;
- Three VBAT_BB pins are used to supply power to baseband of the module.

The following table shows the distribution of the power pins and ground pins of the module:

Table 6 VBAT Pins and Ground Pins

Pin name	Pin number	Description	Min. Value	Typical Value	Max. Value	Unit
VBAT_RF	229, 230, 232, 233	Module RF Power supply	3.3	3.8	4.3	V
VBAT_RF1	107, 109, 110, 112	Module RF Power supply	3.3	3.8	4.3	V
VBAT_BB	235,236,238	Module baseband power supply	3.3	3.8	4.3	V
GND	12, 18, 26, 33, 42, 84, 90, 96, 113, 115, 116, 118, 119, 122-129, 131-134, 136, 137, 140-147, 149, 151, 152, 154-156, 158, 160, 161, 163, 164, 167-170,172, 173, 176-179, 181, 182, 185, 187, 188, 190, 191, 194-197, 200, 202, 203, 205, 206, 209, 211, 212, 214, 215, 224, 226-228,	Ground	-	0	-	V

	231, 234, 299-392,

3.6.2 Reduce Voltage Drop

The power supply range of 5G SRM815 is 3.3V~4.3V. In order to ensure the normal operation of the module, the power supply must have sufficient power supply capability and the input voltage must not be lower than 3.3V. If the supply voltage of VBAT is too low due to an instantaneous voltage drop, the module will be restarted or shut down. The following figure shows the voltage drop during burst transmission in 3G, 4G and 5G network.

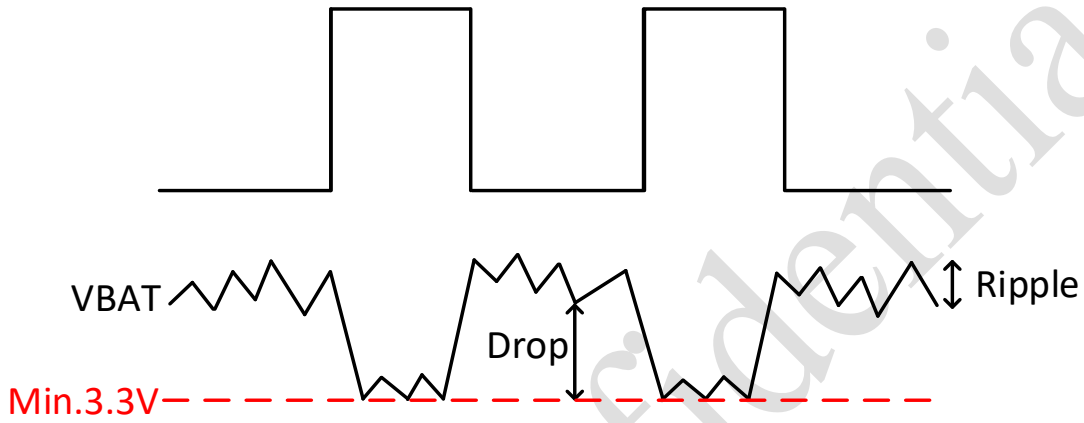

Figure 4 Power Requirements of Burst Transmission

To reduce voltage drop, a 100uF filter capacitor with low ESR is required. Chip multi-layer ceramic capacitor (MLCC) has the best ESR. It is recommended to add 3 ceramic capacitors (100nF, 33pF, 10pF) to VBAT_BB , VBAT_RF and VBAT_RF1 pins, respectively, and the capacitors shall be placed near the VBAT pins. At the same time, in order to ensure better power supply performance, a TVS is added near the VBAT input end of the module to increase the module's bearing capability of surge voltage. When the external power supply is connected to the module, VBAT_BB , VBAT_RF and VBAT_RF1 shall adopt star-shaped routing, and the routing width of each network shall not be less than 2mm. In principle, the longer the VBAT routing, the wider the line is.

The reference circuit of the VBAT input end is as below:

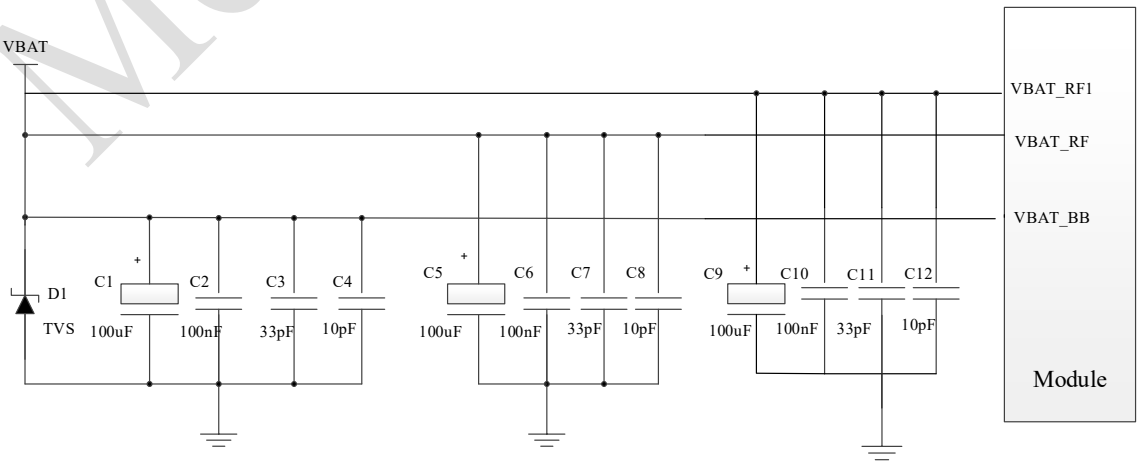

Figure 5 Power Supply Circuit of Module

3.6.3 Power Supply Reference Circuit

The design of module power supply is very important because the performance of the module depends heavily on power supply. 5G SRM815 must choose a power supply capable of providing at least 5A current. If the difference between the input voltage and the supply voltage of the module is not very large, it is recommended to choose LDO as the power supply. If there is a large difference between the input voltage and the output voltage, it is recommended to use DCDC as the power supply for the module.

The following figure shows the reference design of +5V power supply circuit. This design uses DCDC of Silergy Corp., the model is SY8156ADC. Its typical output voltage is 3.8V and the peak load current is up to 5A.

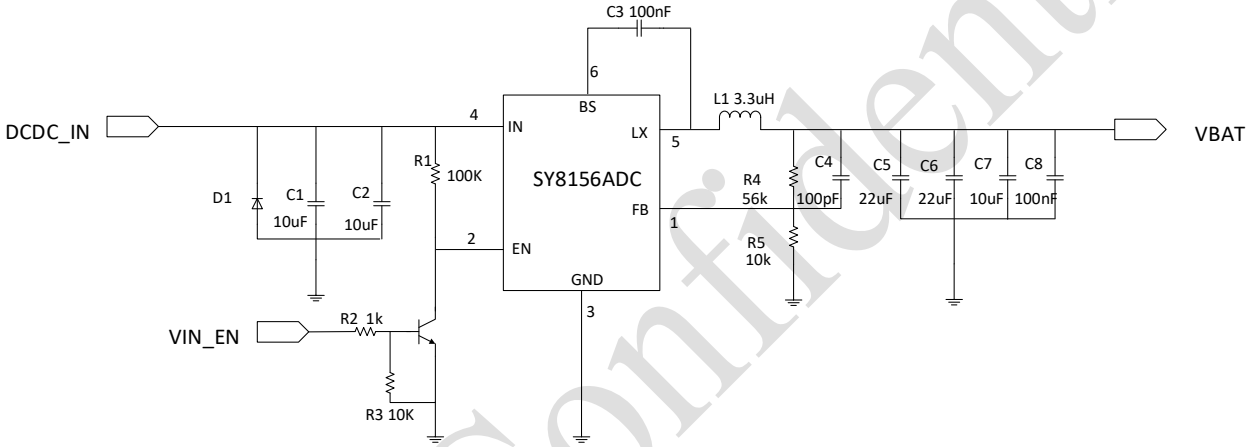

Figure 6 Reference Design of Power Supply Circuit

3.6.4 VREG_L6_1P8 Voltage Output

When 5G SRM815 module is started normally, there is a voltage output on Pin66, the output voltage is 1.8V, and the load current is 50mA. This output voltage can be used for external power supply, such as level reference. At the same time, it can read the level status of the Pin to determine whether the module is started.

3.7 Starting / Shutdown

3.7.1 Starting by PWRKEY Pin

Table 7 PWRKEY Pin Description

Pin Name	Pin Number	Description	DC Features	Remarks
PWRKEY	7	Used for starting / shutdown of the	V_{IH}max=2.1V V_{IH}min=1.3V	Internal pull up

	module	V_{IL}max=0.5V

When 5G SRM815 module is in shutdown mode, the module can be started by pulling down the PWRKEY for at least 100ms. It is recommended to use open-collector drive circuit to control the PWRKEY pin. After the STATUS pin outputs low level, PWRKEY can be released. The reference circuit is as below:

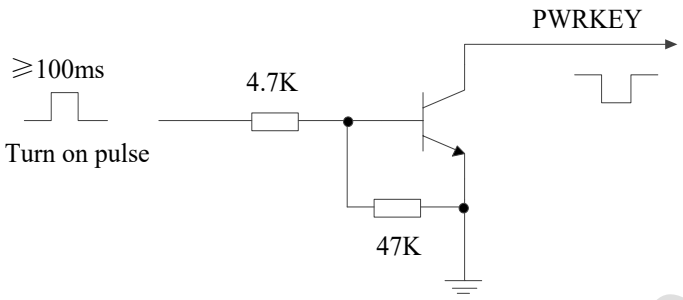

Figure 7 Reference Starting Circuit of Open-Collector Drive

Another way to control PWRKEY pin is to use a button switch directly. A TVS shall be placed near the button for ESD protection. The reference circuit is as below:

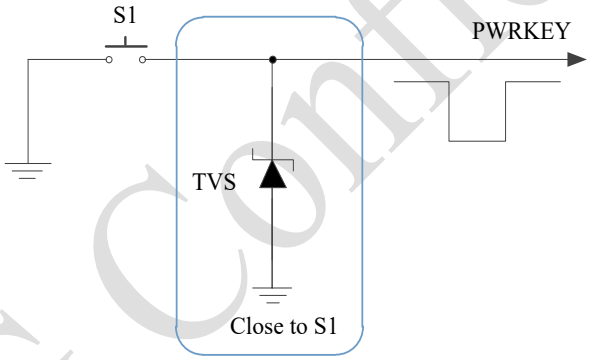

Figure 8 Reference Circuit of Starting By Button

The starting sequence is shown in the following figure:

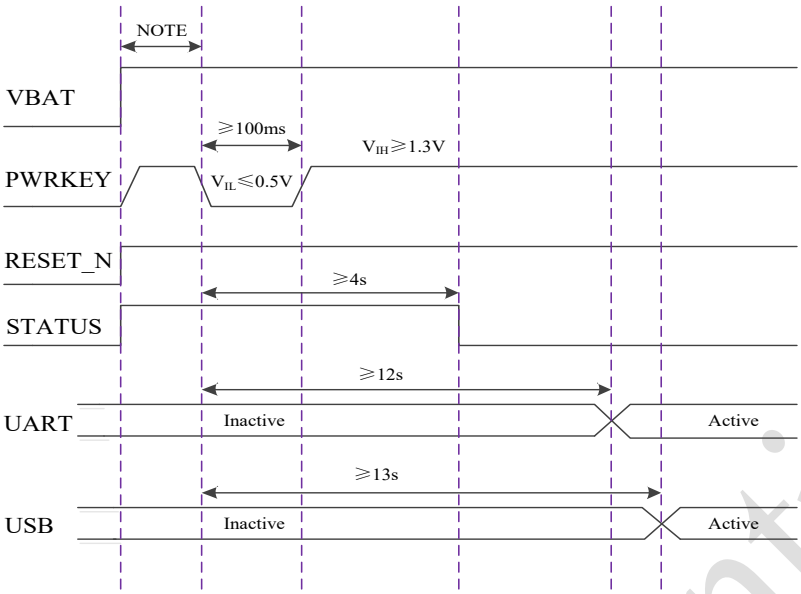

Figure 9 Starting Sequence Diagram

Note:
Before pulling down the PWRKEY pin, ensure that the VBAT voltage is stable. It is recommended that the time interval between powering on VBAT and pulling down PWRKEY pin shall be not less than 30ms.

3.7.2 Shutdown

The module can be shut down in the following ways:

- Normal shutdown: control the module shutdown through the PWRKEY pin;
- Normal shutdown: Control the module shutdown by AT command.

3.7.2.1 Shutdown by AT Command

AT+Poweroff command can be used to control the module shutdown.

3.7.2.2 Shutdown by PWRKEY Pin

When the module is in the starting status, pull down the PWRKEY pin for at least 6.5s and then release it, the module will execute the shutdown process. See the following figure for the shutdown sequence:

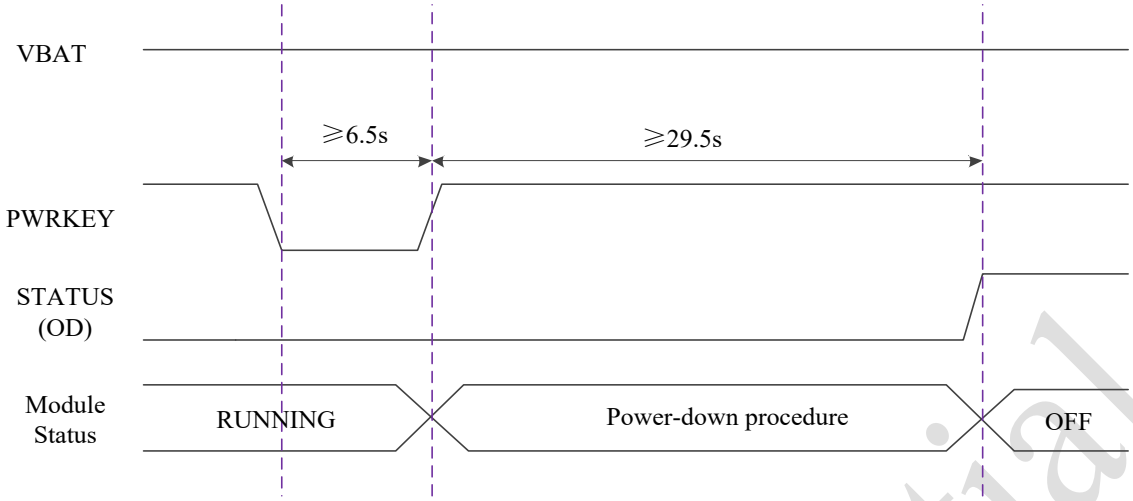

Figure 10 Shutdown Sequence Diagram

Note:

1. When the module is working normally, do not immediately cut off the power supply of the module power, so as not to damage the Flash data inside the module. It is strongly recommended to shut down the module by AT command before powering off.
2. When using AT command to shut down, ensure that the PWRKEY is always at a high level after the shutdown command is executed, otherwise the module will be automatically started again after the shutdown is completed.

3.8 Reset Function

There are two reset modes for 5G SRM815: reset by hardware and reset by AT command.

3.8.1 Reset by Hardware

When the module is working, reset the module by pulling down the RESET_N pin for at least 150ms. RESET_N signal is very sensitive to interference, so it is recommended that the routing on the module interface board should be as short as possible and coated with ground wire.

Table 8 RESET_N Pin Description

Pin Name	Pin Number	Description	DC Features	Remarks
RESET_N	8	Reset module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

The reference circuit is similar to the PWRKEY control circuit. Customers can control RESET_N pin by using open-collector drive circuit or button.

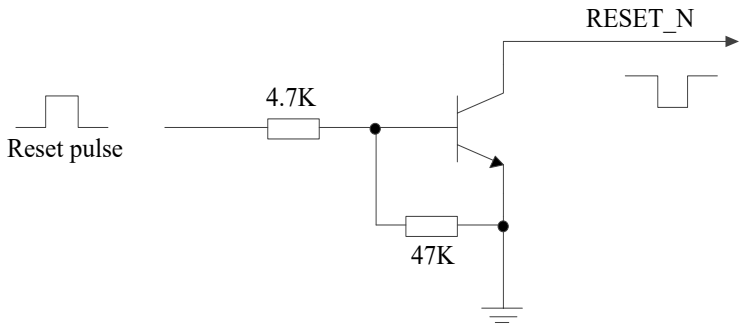

Figure 11 Reference Circuit of RESET_N Reset Open Collector

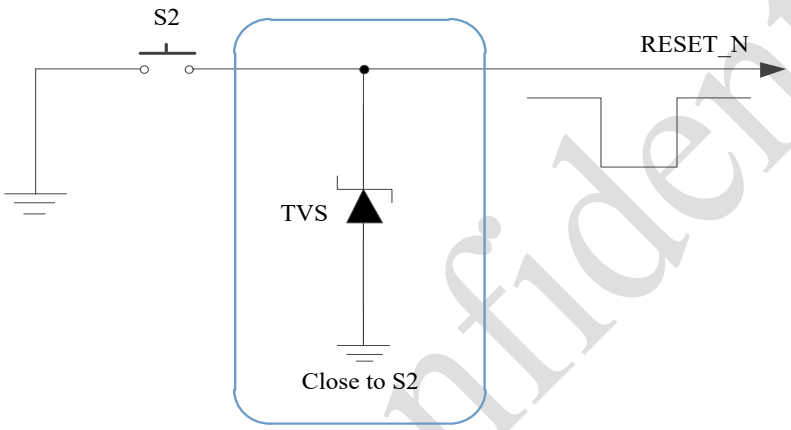

Figure 12 Reference Circuit of RESET_N Reset Button

The reset sequence diagram is as below:

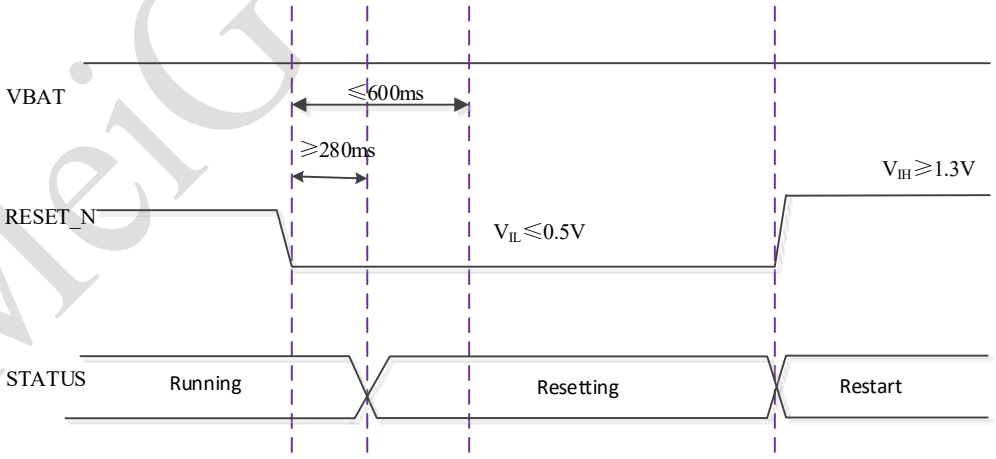

Figure 13 RESET_N Reset Sequence Diagram

3.8.2 Reset by AT Command

Through the 5G SRM815 UART or USB AT port, enter the AT+RESET command to reset and restart the

5G SRM815.

3.9 USIM/SIM Interface

USIM card interface circuit meets the requirements of ETSI and IMT-2000 SIM interfaces. 5G SRM815 supports USIM card of 1.8V and 3.0V.

Table 9 USIM/SIM Interface Description

Pin Name	Pin Number	I/O	Description	Remarks
USIM1_DET	249	DI	USIM card plug detection	It needs to be pulled up to 1.8V
USIM1_VDD	245	PO	USIM card power supply	Support USIM card of 1.8V and 3.0V
USIM1_DATA	248	IO	USIM card data signal	
USIM1_CLK	247	DO	USIM card clock signal	
USIM1_RST	244	DO	USIM card reset signal	
USIM2_DET	252	DI	USIM card plug detection	It needs to be pulled up to 1.8V
USIM2_VDD	250	PO	USIM card power supply	Support USIM card of 1.8V and 3.0V
USIM2_DATA	251	IO	USIM card data signal	
USIM2_CLK	253	DO	USIM card clock signal	
USIM2_RST	254	DO	USIM card reset signal	

5G SRM815 module supports the hot plug function of USIM card through the USIM_DET pin, which supports high-level detection, and the hot plug function is turned off by default. In the figure, after the SIM card is inserted, the USIM_DET pin is at low level. When no card is detected, the USIM_DET pin is at high level.

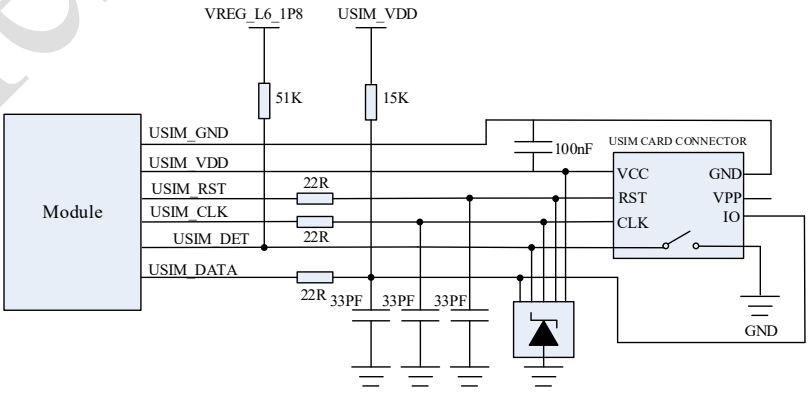

Figure 14 Reference Design Drawing of 8-Pin USIM/SIM Card Connector

If the USIM card detection function is not required, please keep USIM_DET pin unconnected. The following figure shows the reference circuit of 6-pin USIM card connector interface:

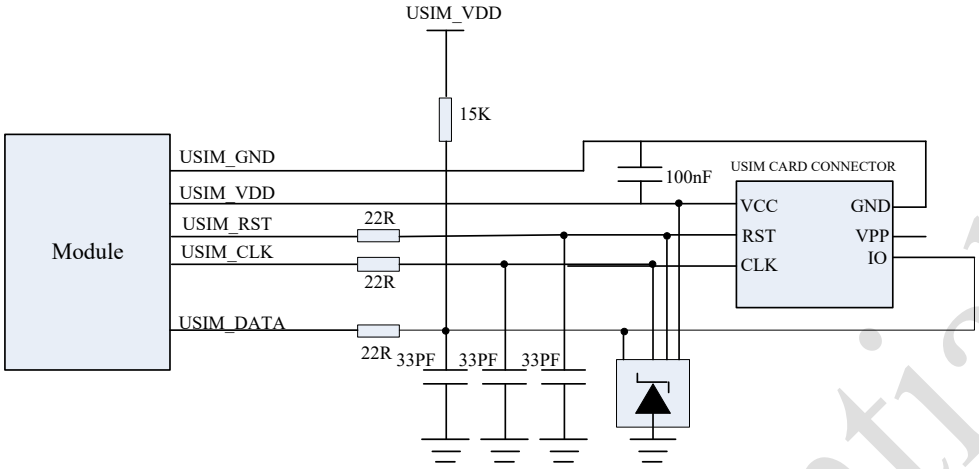

Figure 15 Reference Design Drawing of 6-Pin USIM/SIM Card Connector

In the circuit design of USIM card interface, in order to ensure the good performance and reliability of USIM card, it is recommended to follow the following design principles in circuit design:

- USIM_DATA needs a pull-up resistor to USIM_VDD, this pull-up resistor is 15kΩ; this pull-up resistor is helpful to increase the anti-interference ability of SIM card. When the routing of USIM card is too long or there is an interference source nearby, it is recommended to add a pull-up resistor near the card connector;
- Connect a 22Ω resistor in series to the USIM_DATA, USIM_CLK and USIM_RST circuits, so as to suppress stray EMI, enhance ESD protection and facilitate debugging;
- In order to improve the anti-static ability, add TVS and ESD protective device with parasitic capacitance not greater than 15pF to USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST circuits;
- Connect a 33pF capacitor in parallel to USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST circuits to filter out radio frequency interference; the peripheral parts of USIM card should be placed as close to USIM card connector as possible;
- USIM card connector is placed close to the module, and try best to ensure that the routing length of USIM card signal line does not exceed 200mm;
- Routing of USIM card signal line shall be away from RF lines and VBAT power lines;
- In order to prevent crosstalk interference of USIM_CLK signal and USIM_DATA, routing of the two should not be too close, and ground shield should be added between two lines;
- For the hot plug function of USIM/SIM, use the DETECT pin of the hot plug card slot and the Pin249 or Pin252 pin of the module. The hot plug function is disabled by default, please contact us for more details of this function.

Note:

If SIM Connectors that do not support hot plug are directly used for hot plug of USIM/SIM card, it may damage USIM /SIM card or 5G SRM815 USIM /SIM interface.

3.10 USB Interface

5G SRM815 provides a USB interface that complies with the USB 3.1 Gen2 specifications and supports a theoretical maximum transmission rate of 10Gb/s. This interface is used for AT command interaction, data transmission, software debugging and version upgrade, etc.

3.10.1 USB Pin Description

5G SRM815 module provides one USB3.1 Super-Speed or one USB2.0 High-Speed interface.

Table 10 USB Interface Description

Name	Pin Name	I/O	Description	Remarks
USB_VBUS	82	PI	USB power supply, used for USB detection	Typical value 5.0V
USB_HS_DP	83	IO	USB differential data signal +	90Ω differential impedance is required
USB_HS_DM	85	IO	USB differential data signal -	90Ω differential impedance is required
USB_SS_TX_P	91	AO	USB transmits signal + at high speed	90Ω differential impedance is required
USB_SS_TX_M	89	AO	USB transmits signal - at high speed	90Ω differential impedance is required
USB_SS_RX_P	88	AI	USB receives signal + at high speed	90Ω differential impedance is required
USB_SS_RX_M	86	AI	USB receives signal - at high speed	90Ω differential impedance is required

3.10.2 USB Reference Circuit

USB interface reference circuit of 5G SRM815 module is shown below.

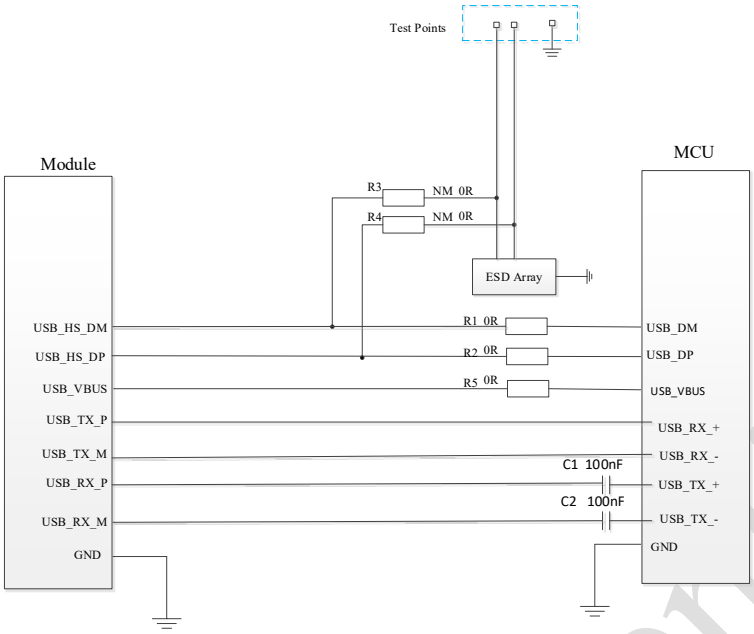

Figure 16 Reference Design Drawing of USB Interface

In order to meet the signal integrity requirement of USB data line, the resistors R1/R2/R3/R4 must be placed close to the module, and the resistors must be placed close to each other. The branch circuit connecting the test points must be as short as possible.

In the design of USB interface circuit, in order to ensure USB performance, it is recommended to follow the following principles in circuit design:

- The module USB_VBUS is not used to supply power to the module, but is used to detect the insertion and removal of USB;
- In order to reduce the signal interference during USB high-speed data transmission, connecting R1 and R2 in series to USB_DM and USB_DP interface circuits can improve the accuracy of data transmission. It is recommended to use 0Ω for both R1 and R2;
- In order to improve the anti-static performance of USB interface, it is recommended to add ESD protective devices to USB_HS_DP, USB_HS_DM, USB_TX_P, USB_TX_M, USB_RX_P and USB_RX_M interface circuits. It is recommended to use ESD devices with the junction capacitance less than 2pF; ESD protective devices for USB should be placed as close to USB interface as possible;
- In order to improve the signal interference during USB3.1 high-speed data transmission, a 100nF capacitor is added to the TX end of MCU to improve the EMI performance.
- In order to ensure the reliable operation of USB, pay more attention to the protection of USB when designing. For example, the protection of USB during Layout requires 90Ω impedance control for USB_HS_DP, USB_HS_DM, USB_TX_P, USB_TX_M, USB_RX_P and USB_RX_M, strictly follow the differential requirements and keep as far away as possible from interference signals when wiring;
- Do not lay USB line under crystal resonator, oscillator, magnetic device and RF signal. It is recommended to use the internal differential routing and coated with ground wire up, down, left and right.

3.10.3 USB Driver

5G SRM815 module supports various operating systems, such as PC operating systems: Windows 7/8, Windows 10, embedded operating systems: Linux 2.6 or higher version, Android2.3/4.0/4.2/4.4/5.0/5.1/6.0/7.0/8.0/9.0/10.0, dedicated USB driver support is required.

USB driver can provide different driver files for different operating systems, different VIDs and PIDs. Please contact support personnel for specific requirements.

3.11 Serial Port

5G SRM815 module has 2 serial ports: Main serial port and debug serial port. The main features of these two serial ports are described below.

- Main serial port supports the baud rates of 9600,19200,38400,57600,115200,230400 and 460800. The default baud rate is 115200bps. It supports RTS and CTS flow control. Used for data transmission and AT command transmission;
- Debug serial port supports the baud rate of 115200bps, used for Linux control and log printing.

Table 11 Pin Description of Main Serial Port

Pin Name	Pin Number	I/O	Description	Remarks
UART1_RXD	70	DI	Module receives data	1.8V power domain
UART1_TXD	68	DO	Module transmits data	1.8V power domain
UART1_DTR	258	DO	Data terminal is ready	1.8V power domain
UART1_RTS	72	DO	Request to send	1.8V power domain
UART1_CTS	69	DI	Clear to send	1.8V power domain
UART1_DCD	261	DI	Data carrier detection	1.8V power domain
UART1_RI	100	DI	Ringing reminder	1.8V power domain

Table 12 Pin Description of Debug Serial Port

Pin Name	Pin Number	I/O	Description	Remarks
DBG_RXD	108	DI	Module receives data	1.8V power domain
DBG_TXD	105	DO	Module transmits data	1.8V power domain

Table 13 Logic Level of Serial Port

Parameter	Minimum value	Maximum Value	Unit

V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The serial level of the 5G SRM815 module is 1.8V. If the client host is 3.3V, a level translator shall be added in serial port application. It is recommended to use TXB0104PWR from TI. The following figure shows the reference design:

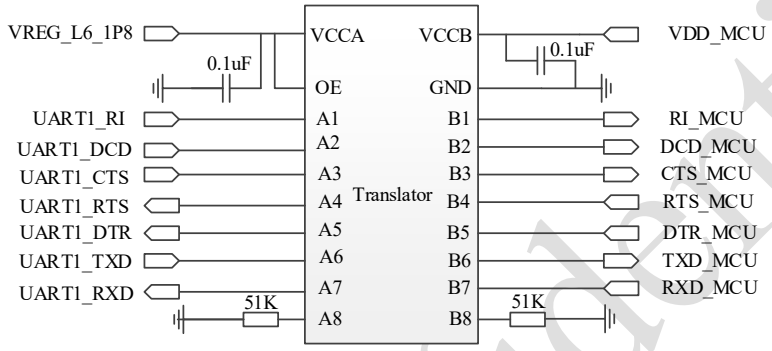

Figure 17 Reference Circuit of Level Translator Chip

3.12 I2S and I2C Interfaces

5G SRM815 provides one I2S interface that supports the following 2 modes:

- Short frame mode: The module can be used as a master unit or slave;
- Long frame mode: The module can only be used as a master unit.

In short frame mode, data is sampled on the falling edge of I2S_SCK and transmitted on the rising edge. The falling edge of I2S_WS represents the most significant bit. I2S_SCK supports 128, 256, 512, 1024 and 2048kHz voice clocks.

In long frame mode, data is sampled on the falling edge of I2S_SCK and transmitted on the rising edge. But the rising edge of I2S_WS represents the most significant bit. In this mode, I2S interface supports only 128 kHz, I2S_SCK and 8kHz, and I2S_WS of 50% duty ratio.

5G SRM815 module supports 8-bit A-law, u-law and 16-bit linear coding formats. The following two figures are the sequence diagram of short frame mode (I2S_WS=8 kHz, I2S_SCK=2048kHz) and the sequence diagram of long frame mode (I2S_WS=8 kHz, I2S_SXK=128kHz), respectively.

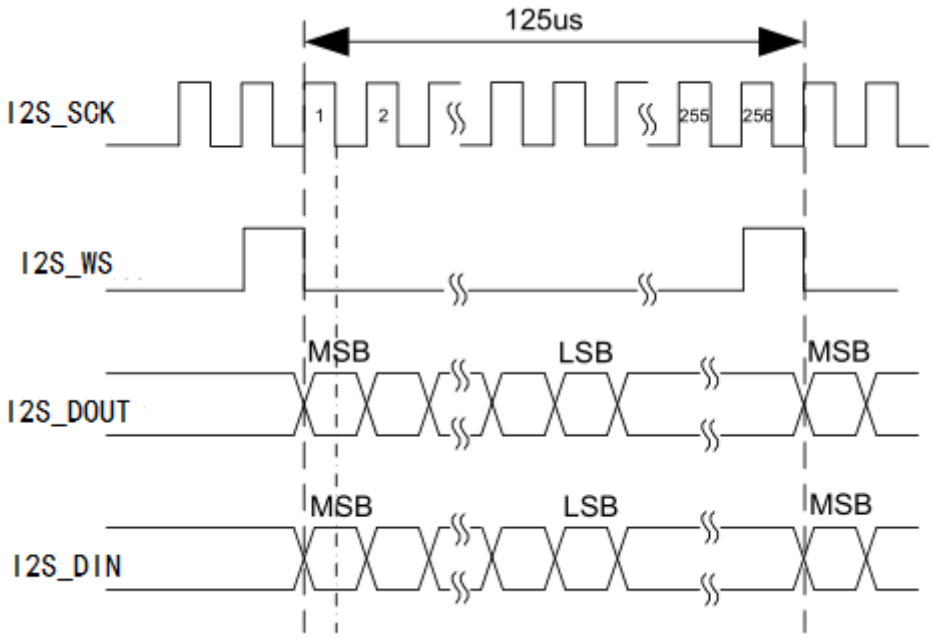

Figure 18 Sequence Diagram of Short Frame Mode

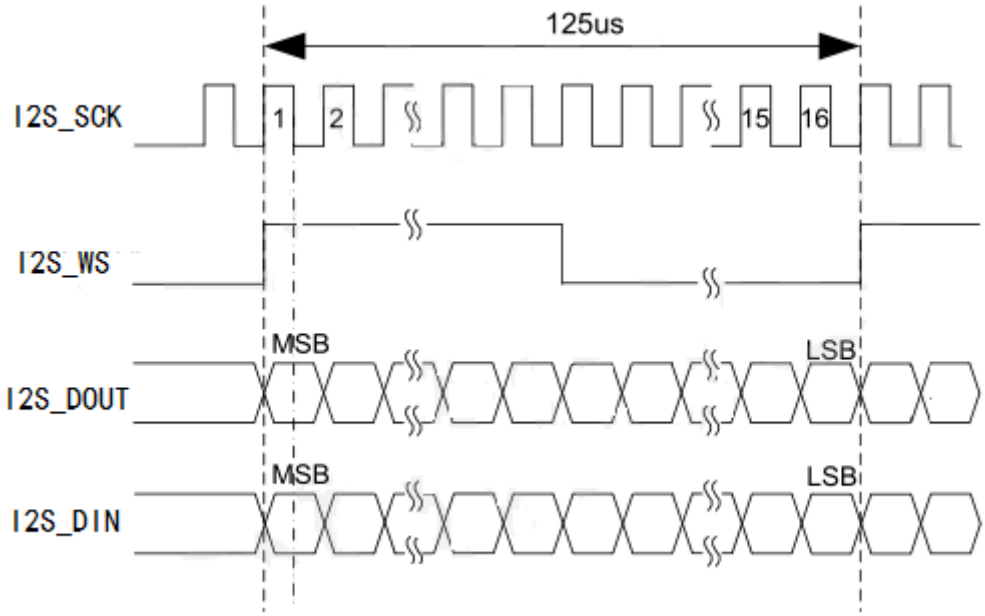

Figure 19 Sequence Diagram of Long Frame Mode

Table 14 I2S Interface Pin Description

Pin Name	Pin Number	I/O	Description	Remarks
I2S_MCLK	79	IO	I2S master clock	1.8V power domain

I2S_SCK	256	IO	I2S clock	1.8V power domain
I2S_DOUT	255	DO	I2S data output	1.8V power domain
I2S_DIN	257	DI	I2S data input	1.8V power domain
I2S_WS	259	IO	I2S data synchronization signal	1.8V power domain
I2C_SCL	77	OD	I2C clock	External 1.8V pull-up is required
I2C_SDA	78	OD	I2C data	External 1.8V pull-up is required

The following figure shows the reference design of I2S interface with external Codec chip:

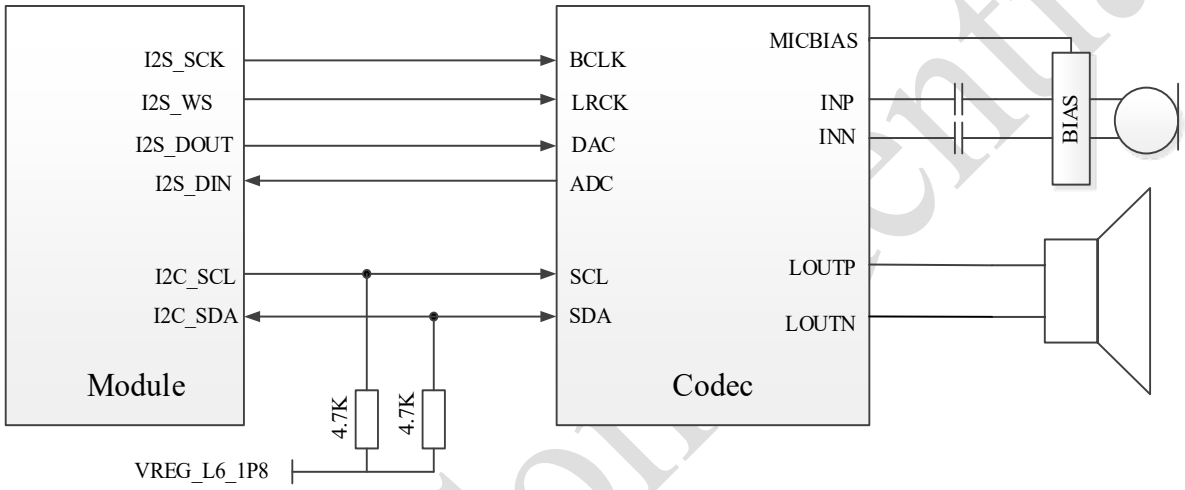

Figure 20 Reference Design of I2S Circuit

3.13 Network Status Indication

Network status indication pin is mainly used to drive the network status indicator (the LED lights are turned on and off by controlling the on and off of the triode to power on or off the LED lights, and the LED lights cannot be driven directly). 5G SRM815 module has two network status pins, NET_MODE and NET_STATUS. The following two tables describe the pin definitions and logic level changes in different network status, respectively.

Table 15 Network Indication Pin Description

Pin Name	Pin Number	I/O	Description	Remarks
NET_MODE	240	DO	Indicate the network registry status of the module	1.8V power domain
NET_STATUS	243	DO	Indicate the network operation status of the module	1.8V power domain

Table 16 Working Status of Network Indication Pin

Modes	Status	Description
NET_MODE	High level	LTE network registry status
	Low level	Other
NET_ STATUS	Flashing (200ms high / 1400ms low)	Data transmission status
	High level	Network registry is finished
	Low level	Other

The reference circuit is shown below:

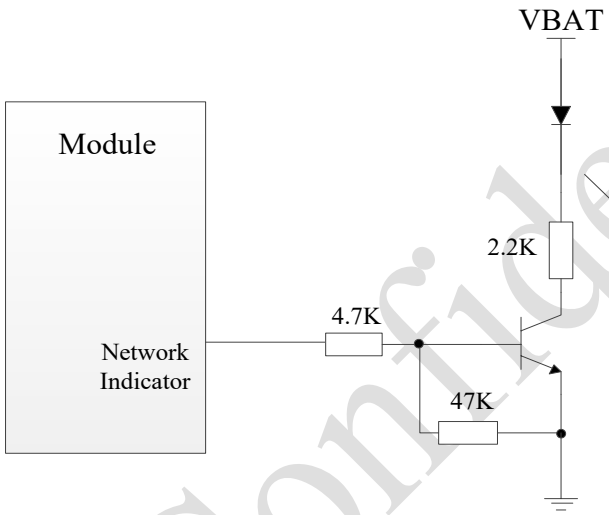

Figure 21 Reference Design Drawing of Network Indication

3.14 STATUS

STATUS is used to indicate the working status of the module. It is an open-drain output pin. Customers can refer to the LED indication circuit shown in the following figure. When the module is started normally, STATUS will output low level. Otherwise, STATUS changes to high impedance status.

Table 17 STATUS Pin Description

Name	Pin Number	Description	I/O	Remarks
STATUS	237	Indicate the working status of module	OD	External pull-up is required

The following figure shows the reference circuit design of STATUS:

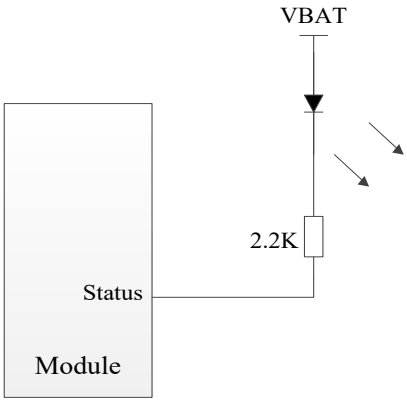

Figure 22 Reference Circuit of STATUS

3.15 ADC Function

5G SRM815 provides 2 analog-to-digital conversion interfaces. Using AT+ADCREAD=1 can read the voltage value of ADC0, and using AT+ ADCREAD =6 can read the voltage value of ADC1.

In order to ensure the accuracy of ADC voltage measurement to be higher, the routing of ADC shall be coated with ground wire.

Table 18 ADC Pin Description

Pin Name	Pin Number	Description	Voltage range
ADC0	241	Analog-to-digital converter interface 0	0-1.875V
ADC1	111	Analog-to-digital converter interface 1	0-1.875V

Note:
1. When the module is not powered by VBAT, ADC interface cannot be directly connected to any input voltage.
2. It is recommended that the ADC pin shall use divider circuit input.

3.16 RGMII Interface

5G SRM815 module includes an integrated Ethernet MAC RGMII interface and two management interfaces (MDIO). The main features of RGMII interface are as follows:

- Comply with IEEE802.3 standard;
- 1000Mbps full duplex;
- 10/100Mbps half / full duplex;

- Support VLAN tag;
- Support IEEE1588 and Precision Time Protocol (PTP);
- It can be used to connect external PHY (such as AR8035) or external exchange;
- MDIO supports 1.8V

Table 19 RGMII Interface Pin Description

Pin Name	Pin Number	Description	I/O	Remarks
RGMII_MDIO	10	RMII MDIO data input/output signal	IO	1.8V power domain
RGMII_MDC	11	RGMII interface clock output	DI	1.8V power domain
RGMII_RX0	13	RGMII interface receives data bit0	DI	1.8V power domain
RGMII_RX1	14	RGMII interface receives data bit1	DI	1.8V power domain
RGMII_CTL_RX	15	RGMII interface receives control signal	DI	1.8V power domain
RGMII_RX2	16	RGMII interface receives data bit2	DI	1.8V power domain
RGMII_RX3	17	RGMII interface receives data bit3	DI	1.8V power domain
RGMII_CK_RX	19	RGMII receives clock signal	DI	1.8V power domain
RGMII_TX0	20	RGMII interface transmits data bit0	DO	1.8V power domain
RGMII_CTL_TX	21	RGMII interface transmits control signal	DO	1.8V power domain
RGMII_TX1	22	RGMII interface transmits data bit1	DO	1.8V power domain
RGMII_TX2	23	RGMII interface transmits data bit2	DO	1.8V power domain
RGMII_CK_TX	24	RGMII interface transmits clock signal	DO	1.8V power domain
RGMII_TX3	25	RGMII interface transmits data bit3	DO	1.8V power domain
RGMII_PWR_EN	27	RGMII power enable control signal	DO	1.8V power domain
RGMII_INT	29	RGMII interrupt signal	DI	1.8V power domain
RGMII_RST	31	RGMII reset signal	DO	1.8V power domain
RGMII_PWR_IN	28	Use an external LDO to provide 1.8V power supply for RGMII_PWR_IN	PI	When the module supports RGMII function, 1.8V power input externally provided is required. When RGMII function is not required, this pin shall be connected to

The following figure shows the application block diagram of Ethernet

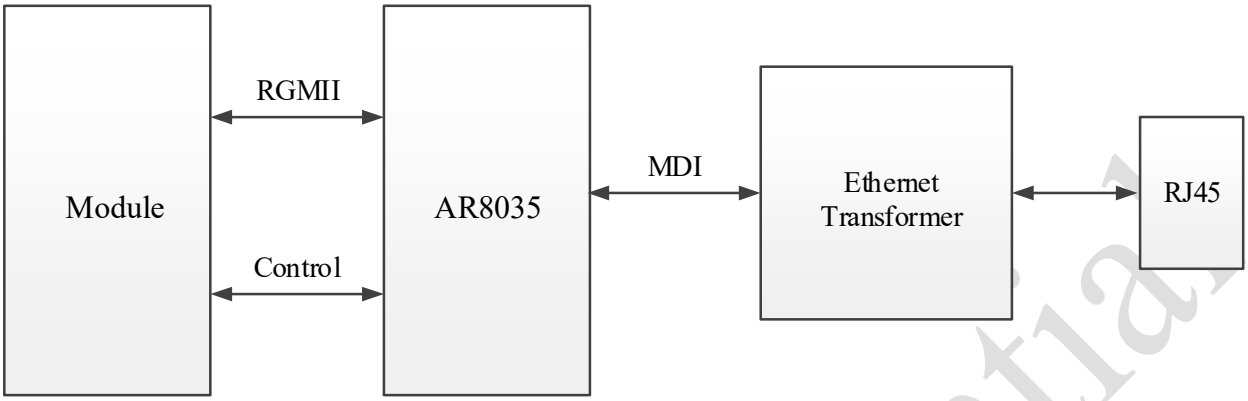

Figure 23 Ethernet Application Diagram

The following figure shows the application reference circuit of the module RGMII and PHY AR8035:

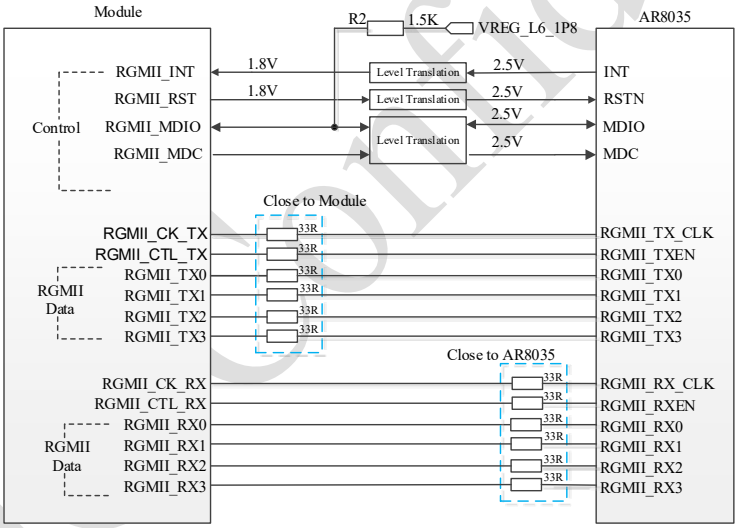

Figure 24 Application Circuit Diagram of RGMII Interface and PHY AR8035

In order to improve the application reliability for customers, please follow the standard Ethernet PHY circuit design. The main points of attention are as follows:

- Keep the data and control signal lines of RGMII away from RF and VBAT when routing;
- The maximum line length shall not exceed 25.4cm, and the length difference between the data lines is controlled at 0.7mm;
- The single-ended impedance of RGMII data line is controlled within 50 Ω±10%, and ensure a complete reference plane;
- The distance between RGMII signal line and other signal lines should be at least 3 times the line width;
- RGMII control signal line requires level translation.

3.17 Wireless Connection Interface

5G SRM815 module provides a separate WIFI module deployment solution for WLAN design.

The pin definition of wireless connection interface is as follows:

Table 20 Pin Description of Wireless Connection Interface

PCIe Part				
Pin Name	**Pin Number**	**Description**	**I/O**	**Remarks**
PCIE_REFCLK_P	40	PCIe differential clock positive signal	AO	85Ω differential impedance control
PCIE_REFCLK_M	38	PCIe differential clock negative signal	AO	
PCIE_TX0_M	44	PCIe transmits negative signal differentially	AO	
PCIE_TX0_P	46	PCIe transmits positive signal differentially	AO	
PCIE_RX0_M	32	PCIe receives negative signal differentially	AI	
PCIE_RX0_P	34	PCIe receives positive signal differentially	AI	
PCIE_CLKREQ	36	PCIe data request signal	IO	
PCIE_RST	39	PCIe reset signal	IO	
PCIE_WAKE	30	PCIe wake-up signal	IO	
Coexistence and control parts				
Pin Name	**Pin Number**	**Description**	**I/O**	**Remarks**
WLAN_PWR_EN2	219	WLAN power enable signal	DO	
WLAN_PWR_EN1	216	WLAN power enable signal	DO	
WLAN_EN	222	WLAN enabled, active high	DO	
COEX_UART_RXD	65	Serial port receiving synchronously	DI	
COEX_UART_TXD	67	Serial port transmitting synchronously	DO	
SLEEP	225	Sleep clock output	DO	
HST_LAA_RX	201	Module controls WLAN 5G LNA to enter isolation mode signal	DO	
HST_AS_EN	159	N79/LAA turns off WLAN 5G signal	DO	
HST_PA_MUTE	162	SDX controls to turn off WLAN PA signal	DO	

HST_LAA_TX_EN	135	N79/LAA controls WLAN 5G PA to enter isolation mode signal	DO
HST_WL_TX_EN	138	WLAN controls N79/LAA signal and turns off the corresponding LNA	DO
SDX_TO_WL_CTI	276	Module controls WLAN signal	DO
SW_CTRL_GPIO	180	Switching control signal	DI
WL_TO_SDX	275	WLAN wakes up module signal	DI

BT part

Pin Name	Pin Number	Description	I/O	Remarks
BT_EN	64	Bluetooth enabled	DO	1.8V power domain, active high
BT_UART_RTS	61	Bluetooth serial port requests to send data	DI	1.8V power domain, not connected when not in use.
BT_UART_TXD	59	Bluetooth serial port transmits data	DO	1.8V power domain
BT_UART_RXD	63	Bluetooth serial port receives data	DI	1.8V power domain
BT_UART_CTS	62	Bluetooth serial port clears to send	DI	1.8V power domain
PCM_IN	74	PCM data input	DI	1.8V power domain
PCM_OUT	76	PCM data output	DO	1.8V power domain
PCM_SYNC	71	PCM data frame synchronization signal	IO	1.8V power domain
PCM_CLK	73	PCM data bit clock	IO	1.8V power domain

The following figure shows the reference diagram of the connection between wireless connection interface and QCA6391 module:

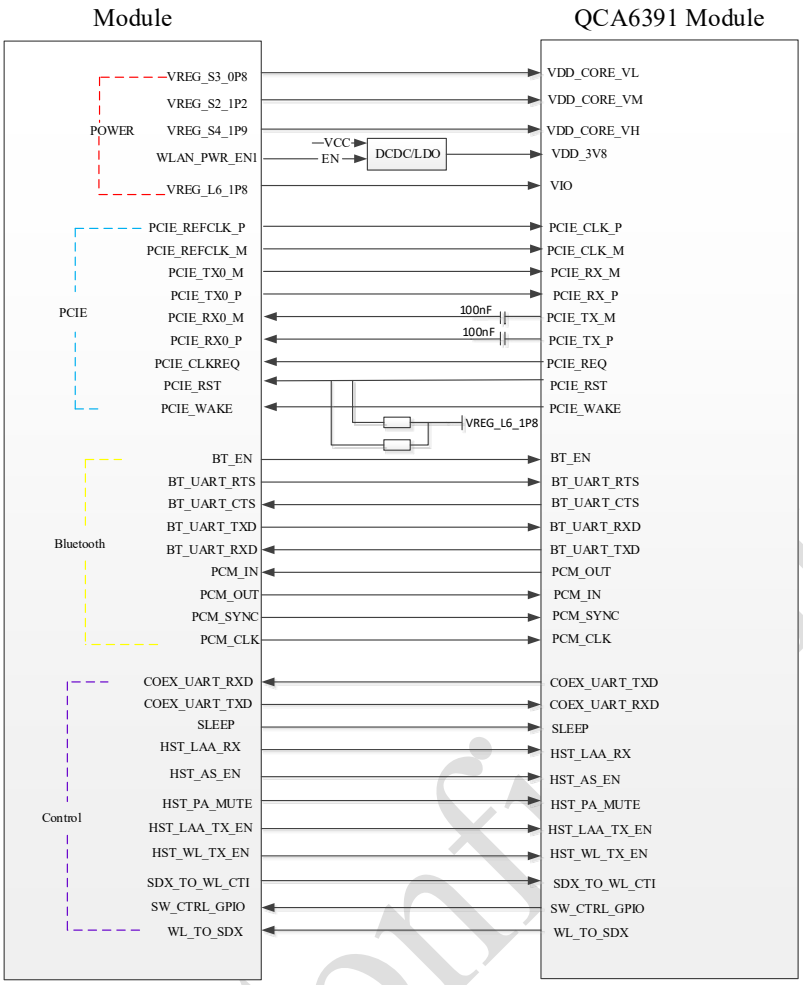

Figure 25 Reference Circuit of the Connection Between Wireless Interface and QCA6391

Note:

1. QCA6391 can only be used as a slave;
2. When 5G SRM815 module has the Bluetooth function enabled, PCM_SYNC and PCM_CLK are only used for signal output;

3.17.1 PCIe Interface

5G SRM815 module provides PCIe Gen3 interface.

The maximum frequency of each lane of PCIe Gen3 is 8Gb/s.

PCIe interface rate is very high. In order to ensure the interface design to be standardized, it is recommended to follow the following principles in circuit design:

- Differential impedance within 85 Ω (±10%) is required for PCIe signal line. It is recommended that the signal line shall be coated with ground wire up, down, left and right;
- PCIe signal line should be kept away from sensitive signals such as RF circuits and analog signals, etc. and noise signals such as clock signals and DCDC, etc.;
- It is recommended to keep the routing length difference between the lines in the module less than 0.7mm;

- A 100nF capacitor is placed near the TX end of the QCA6391 module, and the internal TX output of the module already has a 100nF capacitor, which needn't to be placed at the peripheral circuits.

3.17.2 Bluetooth Interface

5G SRM815 module provides a dedicated UART interface and a PCM interface for Bluetooth interface.

Table 21 Bluetooth Interface Pin Description

Pin Name	Pin Number	Description	I/O	Remarks
BT_EN	139	Bluetooth enabled	DO	1.8V power domain, active high
BT_UART_RTS	61	Bluetooth serial port requests to send data	DI	1.8V power domain, not connected when not in use.
BT_UART_TXD	59	Bluetooth serial port transmits data	DO	
BT_UART_RXD	63	Bluetooth serial port receives data	DI	
BT_UART_CTS	62	Bluetooth serial port clears to send	DO	
PCM_IN	24	PCM data input	DI	
PCM_OUT	25	PCM data output	DO	
PCM_SYNC	26	PCM data frame synchronization signal	IO	
PCM_CLK	27	PCM data bit clock	IO	

3.18 SD Card Interface

SD card interface of 5G SRM815 module supports SDIO 3.0 protocol. The definition of interface pin is as below:

Table 22 SD Card Interface Pin Description

Pin Name	Pin Number	Description	I/O	Remarks
SDIO_VDD	60	SDC1 power domain supply voltage	PI	This voltage is provided externally. According to SD requirements, select input voltage of 1.8V or 2.85V. When not in use, this pin shall be connected to VREG_L6_1P8(66Pin)
SDC1_CMD	33	SD card SDIO bus command signal	IO	SDIO signal level can be selected according to the signal level supported by SD card. Please refer to SD3.0 protocol for

				details. Not connected when not in use.
SDC1_CLK	32	SD card SDIO bus clock signal	DO	Same as above
SDC1_DATA_0	31	SD card SDIO bus DATA0	IO	Same as above
SDC1_DATA_1	30	SD card SDIO bus DATA1	IO	Same as above
SDC1_DATA_2	29	SD card SDIO bus DATA2	IO	Same as above
SDC1_DATA_3	28	SD card SDIO bus DATA3	IO	Same as above
SD_INS_DET	55	SD card insertion detection	DI	1.8V power domain Not connected when not in use.

Note: SDC1_DATA_5 is used as SD_INS_DET in SD card circuit.

The following figure shows the reference design of SD card:

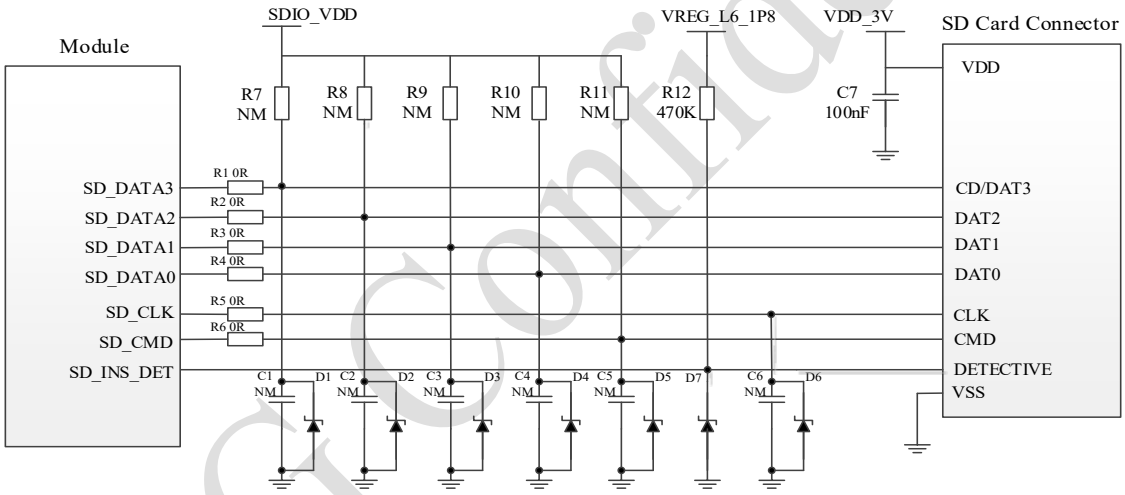

Figure 26 Reference Design Drawing of SD Card

In the circuit design of SD card interface, in order to ensure the good performance and reliability of SD card, it is recommended to follow the following principles in circuit design:

- SD card power needs to be supplied from the outside of the module. The voltage range of VDD_3V is 2.7~3.6V, and at least 800mA current shall be supplied. And use SDIO_VDD to pull up the SDIO bus, SDIO_VDD needs to supply at least 300mA current;
- In order to prevent the current fluctuation when SD card is inserted exceeding the maximum limit, the bypass capacitor C7 of SD card power supply should be less than 5uf;
- To avoid bus jitter, SDIO signal needs to be pulled up to SDIO_VDD through R7~R11 resistors. The resistance of these resistors are 10~100KΩ, and the recommended resistance is 100KΩ;
- In order to adjust the signal quality, it is necessary to reserve SDIO signal series resistors R1~R6, and the recommended resistance is 22Ω; reserve capacitors C1~C6, which are not attached by default. The resistors and capacitors shall be placed close to the module;

- In order to better prevent static electricity, it is recommended to add a TVS to the Pin of SD card; and place it as close to the SD card connector as possible, and ensure that the inter-electrode capacitance of the TVS is less than 15pF;
- SDIO signal line shall be coated with ground wire three-dimensionally, and the impedance is controlled at 50Ω (±10%);
- SDIO signal line should be kept away from sensitive signals such as RF and analog signals, etc. and noise signals such as clock signals and DCDC, etc.;
- It is recommended to keep the routing length difference between CLK and DATA/CMD less than 1mm and the total length less than 50mm. The routing length inside the module is 27mm, so the external routing length should be less than 23mm;
- Ensure that the distance between adjacent lines is twice the routing width, and the bus load is less than 15pF.

3.19 USB_BOOT Interface

5G SRM815 supports USB_BOOT function. Customers can pull up USB_BOOT to VREG_L6_1P8(1.8V) before the module is started, and the module will enter the forced download mode when it is started again. In this mode, the module can conduct software upgrade through USB interface.

Table 23 USB_BOOT Pin Definition

Pin Name	Pin Number	I/O	Description	Voltage Range
USB_BOOT	81	DI	Emergency download mode control, active high	1.8V power domain, it is recommended to reserve test points; not connected when not in use.

The reference circuit of USB_BOOT interface is as below:

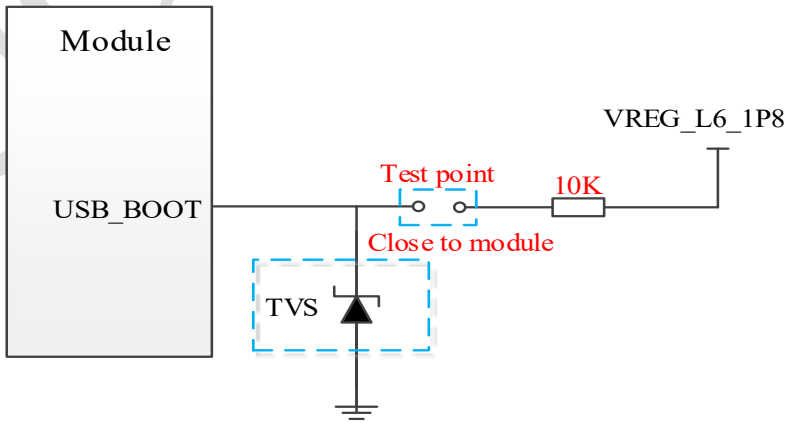

Figure 27 Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1 Basic Description

5G SRM815 includes a complete embedded GNSS solution that supports Qualcomm Gen8C-Lite (GPS, GLONASS, Galileo and BeiDou), and two GNSS channels that support L1 and L5.

5G SRM815 module supports standard NMEA-0183 protocol and outputs 1Hz NMEA sentences through USB interface by default.

4.2 GNSS Performance (TBD)

The following table lists the GNSS performance of 5G SRM815 module.

Table 24 GNSS Performance

Parameter	Description	Performance Index
Positioning accuracy (open area)	CEP-50	TBD
Time to first fix TTFF (open area)	Cold start	TBD
	Warm start	TBD
	Hot Start	TBD
Sensitivity	Cold start	TBD
	Capture	TBD
	Track	TBD

4.3 Layout Guidelines

During design, customers should follow the following layout guidelines:

- The distance between each antenna should be as large as possible;
- Digital signals such as USIM card, USB interface, camera module, display interface and SD card should be kept away from antenna;
- Sensitive analog signals should be far away from GNSS signal path, and ground holes should be added for isolation and protection;
- ANT_GNSS routing keeps 50Ω characteristic impedance;
- In case of any static electricity or lightning strikes, reserve a place for TVS on the backplane.

Refer to Chapter 5 for GNSS reference design and antenna considerations.

5 Antenna Interface

5G SRM815 module has four 5G antenna interfaces, two 4G antenna interfaces, two MIMO antenna interfaces and one GNSS antenna interface. The impedance of antenna interface is 50Ω.

Table 25 Definition of Antenna Interface Pin

Pin Name	Pin Number	Description	I/O	Remarks
ANT0	121	LMHB TRX n41 TRX1 n79 DRX1	IO	50Ω impedance
ANT1	130	LMHB DRX n41 DRX1 n79 TRX1	IO	50Ω impedance
ANT2	139	n79 DRX0	AI	50Ω impedance
ANT3	148	n79 TRX0	AI	50Ω impedance
ANT4	157	MHB PRX_MIMO n77/78 TRX0 UHB TRX	IO	50Ω impedance
ANT5	166	n77/78 TRX1 n41 TRX0 UHB TRX1	AI	50Ω impedance
ANT6	175	MHB DRX_MIMO n77/78 DRX0 n41 DRX0 UHB DRX	AI	50Ω impedance
ANT7	184	n77/78 DRX1 UHB DRX1	AI	50Ω impedance
ANT_GNSS	193	GNSS antenna interface	AI	50Ω impedance

5.1 Introduction to Antenna Interfaces

5G SRM815 provides 9 antenna pins, including: ANT0, ANT1, ANT2, ANT3, ANT4, ANT5, ANT6, ANT7 and ANT_GNSS. You can choose to connect diversity antenna to improve the 5G NR/LTE/WCDMA receptivity It is recommended that the users use the antenna of 50Ω impedance matching the RF connector on the module.

Note:
In order to ensure the communication capability of all frequency bands, please connect both the main and auxiliary antennas.

It is recommended to carefully select RF patch cord for application side. You need to choose the RF patch

cord with as little loss as possible. It is recommended to use the RF patch cord with the following RF loss requirements:

- 5G NR<1.5dB；
- TDD-LTE<1.5dB;
- FDD-LTE<1.5dB;
- WCDMA<1.5dB;

5.2 RF Reference Circuit

The reference design circuit of 4G, 5G and MIMO antenna connection is shown in the following figure. In order to obtain better RF performance, pay attention to the following four points in schematic diagram design and PCB layout:

1. In schematic diagram design, reserve π-type matching circuit near the RF port of the module, and the capacitor is not attached by default;
2. In schematic diagram design, provide redundant RF connector from the module RF port to antenna, used for certification testing, the RF connector may not be attached after mass production and delivery;
3. In schematic diagram design, reserve π-type matching circuit near the antenna and the capacitor is not attached by default;
4. In PCB layout, the routing from the module RF port to antenna is as short as possible, and the board factory shall make 50Ω impedance control on RF routing.

Note:
Customers need to consider the impedance matching between backplane and module. The reserved matching should be optimized according to the actual situation to ensure the optimum performance.

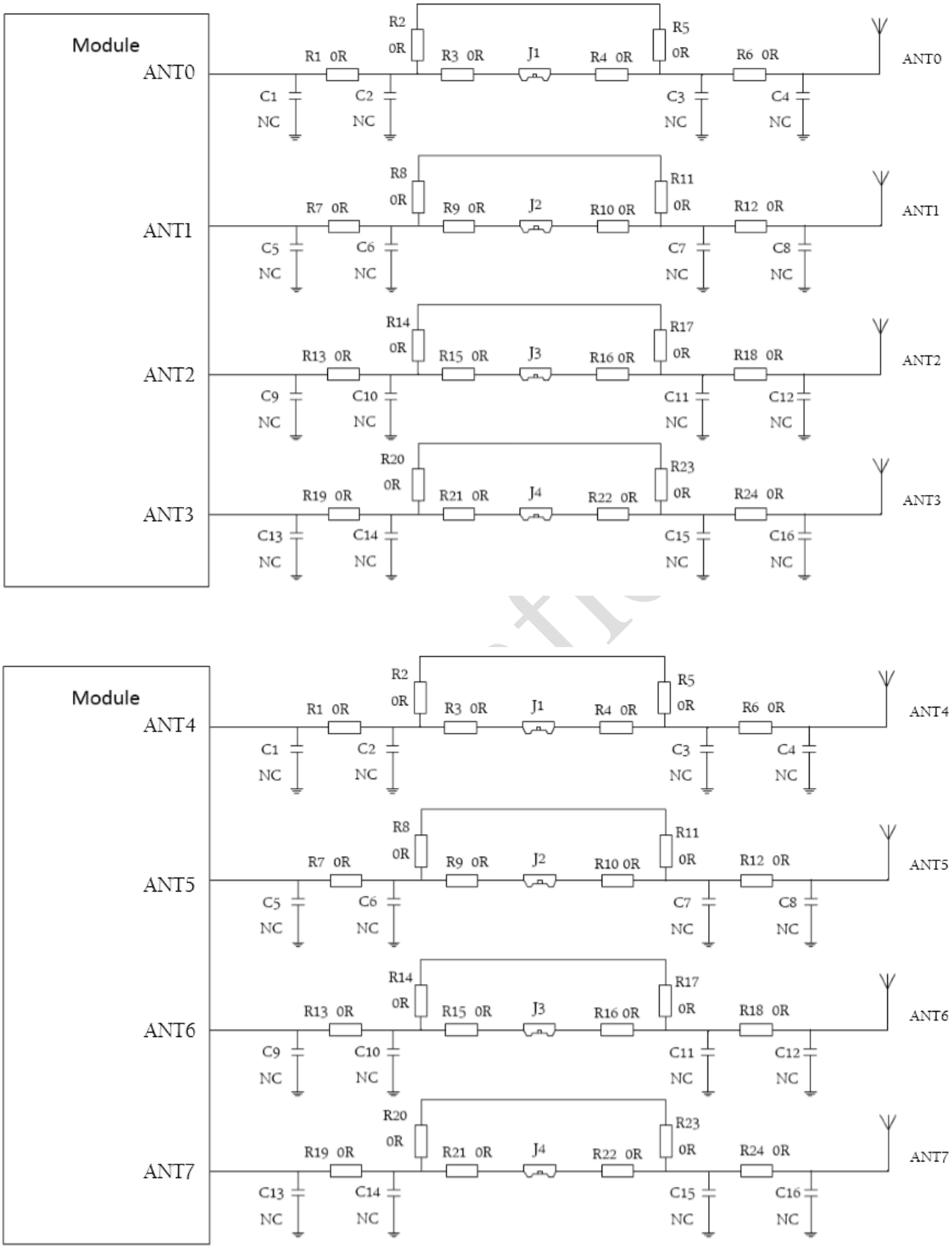

Figure 28 RF Reference Circuit

The reference design of GNSS antenna is shown in the following figure:

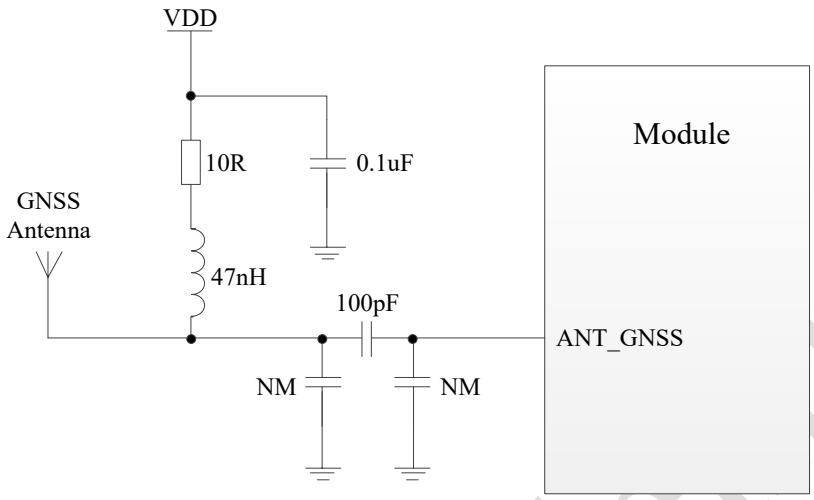

Figure 29 Reference Circuit of GNSS Antenna

Note:

1. Customers can choose external LDO power supply according to the type of active antenna.
2. If the customers use passive antenna, it is not necessary to design VDD circuit.

5.3 Antenna Installation

5.3.1 Antenna Requirements

The requirements for the main antenna, diversity receiving antenna and GNSS antenna are shown in the following table:

Table 26 Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1160MHz-1185MHz 1561 MHz -1615MHz
	Polarization: RHCP or linear
	VSWR: < 2 (typical value)
	Passive antenna gain: > 0 dBi
	Active antenna noise factor: < 1.5 dB
	Active antenna gain: >-2 dBi
	Active antenna embedded LNA gain: 18.5dB (typical value)
	Active antenna total gain: > 18.5 dB (typical value)
WCDMA/TD-SCDMA/CDMA /TDD-LTE/FDD-LTE/5G NR	VSWR: < 2
	Gain (dBi): 1
	Maximum input power (W): 2W

	Input impedance (ohm): 50
	Polarization type: vertical
	Cable insertion loss: < 1.5dB (WCDMA B5/B8, LTE B5/B8/B12/B13/B14/B18/B19/B20/B26/B28/B71,5G N28)
	Cable insertion loss: < 1.5 dB (WCDMA B1/B2/B3/B4, LTE B1/B2/B3/B4/B25/B32/B30/B66)
	Cable insertion loss: < 2dB (LTE B7/B34/B38/B39/B40/B41/B42/B43/B48, 5G N41/N77/N78/N79)

5.3.2 RF Output Power

RF output power of 5G SRM815 is shown in the following table.

Table 27 5G SRM815-EA RF Emission Power

Frequency	Maximum Value	Minimum Value
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B3	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2.7dB	<-39dBm
LTE-FDD B3	23dBm±2.7dB	<-39dBm
LTE-FDD B5	23dBm±2.7dB	<-39dBm
LTE-FDD B7	23dBm±2.7dB	<-39dBm
LTE-FDD B8	23dBm±2.7dB	<-39dBm
LTE-FDD B18	23dBm±2.7dB	<-39dBm
LTE-FDD B19	23dBm±2.7dB	<-39dBm
LTE-FDD B20	23dBm±2.7dB	<-39dBm
LTE-FDD B28	23dBm±2.7dB	<-39dBm
LTE-TDD B34	23dBm±2.7dB	<-39dBm
LTE-TDD B38	23dBm±2.7dB	<-39dBm
LTE-TDD B39	23dBm±2.7dB	<-39dBm
LTE-TDD B40	23dBm±2.7dB	<-39dBm
LTE-TDD B41	23dBm±2.7dB	<-39dBm
LTE-TDD B42	23dBm±2.7dB	<-39dBm
N28	23dBm+2/-2.5dB	<-40dBm
N41	26dBm+2/-3dB	<-33dBm
N77	26dBm+2/-3dB	<-33dBm
N78	26dBm+2/-3dB	<-33dBm
N79	26dBm+2/-3dB	<-33dBm

Table 28 5G SRM815-NA RF Emission Power

Frequency	Maximum Value	Minimum Value
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2.7dB	<-39dBm
LTE-FDD B4	23dBm±2.7dB	<-39dBm
LTE-FDD B5	23dBm±2.7dB	<-39dBm
LTE-FDD B12	23dBm±2.7dB	<-39dBm
LTE-FDD B13	23dBm±2.7dB	<-39dBm
LTE-FDD B14	23dBm±2.7dB	<-39dBm
LTE-FDD B25	23dBm±2.7dB	<-39dBm
LTE-FDD B26	23dBm±2.7dB	<-39dBm
LTE-FDD B28	23dBm±2.7dB	<-39dBm
LTE-FDD B30	23dBm±2.7dB	<-39dBm
LTE-FDD B66	23dBm±2.7dB	<-39dBm
LTE-FDD B71	23dBm±2.7dB	<-39dBm
LTE-TDD B41	23dBm±2.7dB	<-39dBm
LTE-TDD B42	23dBm±2.7dB	<-39dBm
LTE-TDD B43	23dBm±2.7dB	<-39dBm
LTE-TDD B48	23dBm±2.7dB	<-39dBm
N41	26dBm+2/-3dB	<-33dBm
N77	26dBm+2/-3dB	<-33dBm
N78	26dBm+2/-3dB	<-33dBm

5.3.3 RF Receiving Sensitivity

Table 29 5G SRM815-EA Module RF Receiving Sensitivity

Frequency	Receiving sensitivity (typical value) -10M			
	Main	Diversity	Main + Diversity	Standard (Main + Diversity)
WCDMA B1	-108	-112	-113	-108
WCDMA B3	-109	-111	-112	-108
WCDMA B5	-111	-112	-113.5	-108
WCDMA B8	-111	-112	-113.5	-108
LTE-FDD B1	-94	-100	-100.5	-97.3
LTE-FDD B3	-97	-100	-100.5	-97.3
LTE-FDD B5	-98	-101	-101.5	-97.3
LTE-FDD B7	-96	-99	-100	-95.3
LTE-FDD B8	-98	-101	-102	-97.3
LTE-FDD B18	-98	-101	-102	-97.3
LTE-FDD B19	-98	-101	-102	-97.3
LTE-FDD B20	-98	-101	-102	-97.3
LTE-FDD B28	-98	-101	-102	-97.3

LTE-FDD B32	-99	-100	-102	-97.3
LTE-TDD B34	-99	-100	-102	-97.3
LTE-TDD B38	-95	-98	--99	-96.3
LTE-TDD B39	-99	-100	-102	-97.3
LTE-TDD B40	-97	-99	-100	-96.3
LTE-TDD B41	-96	-98	-99	-95.3
LTE-TDD B42	-96	-97	-98.5	-96.3
N28	-98	-101	-102	-95.6(10M)
N41	-86	-88	-89	-87.7(100M)
N77	-85	-85	-87.5	-85.2(100M)
N78	-85	-85	-87.5	-85.7(100M)
N79	-83	-85	-86	-85.7(100M)

Table 30 5G SRM815-NA* Module RF Receiving Sensitivity(TBD)

Frequency	Receiving sensitivity (typical value) -10M			
	Main	Diversity	Main + Diversity	Standard (Main + Diversity)
WCDMA B2				-108
WCDMA B4				-108
WCDMA B5				-108
LTE-FDD B2				-97.3
LTE-FDD B4				-97.3
LTE-FDD B5				-97.3
LTE-FDD B12				-97.3
LTE-FDD B13				-97.3
LTE-FDD B14				-97.3
LTE-FDD B25				-97.3
LTE-FDD B26				-97.3
LTE-FDD B28				-97.3
LTE-FDD B29				-97.3
LTE-FDD B30				-97.3
LTE-FDD B66				-97.3
LTE-FDD B71				-97.3
LTE-TDD B41				-95.3
LTE-TDD B42				-96.3
LTE-TDD B43				-96.3
LTE-TDD B48				-96.3
N41				-95.5(10M) -87.7(100M)
N77				-96(10M) -85.2(100M)
N78				-96.5(10M) -85.7(100M)

5.3.4 Working Frequency

Table 31 5G SRM815-EA Working Frequency

Frequency band	Transmit	Receive	Unit
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B3	1710~1785	1805~1880	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-FDD B18	815~830	860~875	MHz
LTE-FDD B19	830~845	875~890	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B28	703~748	758~803	MHz
LTE-FDD B32	NC	1452~1496	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz
LTE-TDD B42	3400~3600	3400~3600	MHz
N28	703~748	758~803	MHz
N41	2496~2690	2496~2690	MHz
N77	3300~4200	3300~4200	MHz
N78	3300~3800	3300~3800	MHz
N79	4400~5000	4400~5000	MHz

Table 32 5G SRM815-NA Working Frequency

Frequency band	Transmit	Receive	Unit
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE-FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B12	699~716	729~746	MHz
LTE-FDD B13	777~787	746~756	MHz
LTE-FDD B14	788~798	758~768	MHz
LTE-FDD B25	1850~1915	1930~1995	MHz
LTE-FDD B26	814~849	859~894	MHz

LTE-FDD B28	703~748	758~803	MHz
LTE-FDD B29	NC	717~728	MHz
LTE-FDD B30	2305~2315	2350~2360	MHz
LTE-FDD B66	1710~1780	2110~2200	MHz
LTE-FDD B71	663~698	617~652	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz
LTE-TDD B42	3400~3600	3400~3600	MHz
LTE-TDD B43	3600~3800	3600~3800	MHz
LTE-TDD B48	3550~3700	3550~3700	MHz
N41	2496~2690	2496~2690	MHz
N77	3300~4200	3300~4200	MHz
N78	3300~3800	3300~3800	MHz

5.3.5 Antenna Requirements

Table 33 Requirements for Antenna Index

Network Mode	Band	VSWR	Gain		Effi.	SAR	TRP (dBm)	TIS (dBm)
			Peak	Avg.				
WCDMA	Band1						19	<-104
	Band2						19	<-104
	Band3						19	<-104
	Band4						19	<-104
	Band5						18	<-103
	Band8						18	<-103
TDD-LTE(10M)	Band34						19	<-93.5
	Band38						19	<-92.5
	Band39						19	<-93.5
	Band40						19	<-92.5
	Band41						19	<-91.5
	Band42	<2.5:1	>0dBi	>-4dBi	>40%	<1.6W/Kg	19	<-92.5
	Band43						19	<-92.5
	Band48						19	<-92.5
FDD-LTE(10M)	Band1						19	<-93.5
	Band2						19	<-93.5
	Band3						19	<-93.5
	Band4						19	<-93.5
	Band5/26						18	<-92.5
	Band7						19	<-91.5
	Band8						18	<-92.5
	Band12						17	<-92.5
	Band13						17	<-92.5

	Band14	17	<-92.5
	Band18	18	<-92.5
	Band19	18	<-92.5
	Band20	18	<-92.5
	Band25	19	<-93.5
	Band26	18	<-92.5
	Band28	17	<-92.5
	Band30	19	<-93.5
	Band32	19	<-93.5
	Band66	19	<-93.5
	Band71	16	<-92.5
5G NR	N28	18.5	<-90.5(10M)
	N41	18.5	<-91.5(10M)
	N77	18.5	<-92.5(10M)
	N78	18.5	<-92.5(10M)
	N79	18.5	<-82(100M)

Table 34 Requirements for Diversity Antenna Index

Mode	Band	VSWR	Gain /Avg.	Efficiency ρ	Isolation
WCDMA	Band1	<2.5:1	>-7dBi	>20%	Low frequency<0.3 High frequency<0.5	<-8dB
	Band2					
	Band3					
	Band4					
	Band5					
	Band8					
TDD-LTE(10M)	Band34					
	Band38					
	Band39					
	Band40					
	Band41					
	Band42					
	Band43					
	Band48					
FDD-LTE(10M)	Band1					
	Band2					
	Band3					
	Band4					
	Band5/26					

	Band7
	Band8
	Band12
	Band13
	Band14
	Band18
	Band19
	Band20
	Band25
	Band28
	Band30
	Band32
	Band66
	Band71
5G NR(100M)	N28
	N41
	N77
	N78
	N79

6 Electrical Characteristics

6.1 Limiting Voltage Range

Limiting voltage range refers to the maximum voltage range that the module supply voltage and the digital and analog input / output interfaces can withstand. Working outside this range may cause damage to this product.

The limiting voltage range of 5G SRM815 is shown in the following table.

Table 35 Limiting Working Voltage Range of the Module

Parameter	Description	Minimum	Typical	Maximum	Unit
VBAT	5G SRM815 power supply	3.3	3.8	4.3	V
	RMS average supply current	0	0.9	3	A
USB_VBUS	USB detection	3.0	5.0	5.25	V
GPIO	Digital IO level supply voltage	-0.3	1.8	2.0	V
	Supply voltage in shutdown mode	-0.25		0.25	V

6.2 Ambient Temperature Range

5G SRM815 module is recommended to work in -30~+75℃. It is recommended that the application side shall take temperature control measures in harsh environmental conditions. At the same time, it provides the extended working temperature range of the module. When used at the extended temperature, its function is normal, some RF indices may deteriorate. At the same time, it is recommended that the module application terminal be stored under certain temperature conditions. Modules may not work properly or be damaged if exceeding this range.

Table 36 Temperature Range of the Module

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-30	+25	+75	℃
Extended working temperature	-40~-30		+75~+85	℃
Storage temperature	-45		+90	℃

6.3 Electrical Characteristics of Interface in Working Status

V_L: logic low;

V_H: logic high.

Table 37 Logic Levels of Ordinary Digital IO Signals

Signals	V_L		V_H		Unit
	Minimum	Maximum	Minimum	Maximum	
Digital input	-0.3	0.3*Vpin_min	0.3*Vpin_max	Vpin_max	V
Digital output	GND	0.2	Vpin_min-0.2	Vpin	V

Note:
Vpin_min=1.45V, Vpin_max=2.0V (Vpin is the high level of digital interface, Vpin=1.8V)

Table 38 Electrical Characteristics of Power Supply in Working Status

Parameter	I/O	Minimum	Typical	Maximum	Unit
VBAT	I	3.3	3.8	4.3	V
USIM_VDD	O	1.7/2.75	1.8/2.85	1.9/2.95	V

6.4 Power Consumption Range of the Module (TBD)

The following is the power consumption of 5G SRM815 module in each working mode. For more information on frequency band, please contact us.

Table 39 Power Consumption (TBD)

6.5 Environmental Reliability Requirements

Table 40 Environmental Reliability Requirements

Test Item	Test Conditions
Low temperature storage test	Temperature -45℃, 24 hours in shutdown status
High temperature storage test	Temperature +90℃, 24 hours in shutdown status
Thermal shock test	In shutdown status, 1h at the temperature -45℃ and +90℃ respectively. Temperature changeover time <3min, 24 cycles in total
High temperature and high humidity test	Temperature +85℃, humidity 95%RH, 48 hours in shutdown status
Low temperature operation test	Temperature -40℃, 24 hours in working status
High temperature operation test	Temperature +85℃, 24 hours in working status

Test Item	Test Conditions
Vibration test	Perform vibration test according to the requirements shown in the following table: Frequency: Random vibration ASD (Acceleration Spectral Density) 5~20Hz: 0.96m²/s³ 20~500Hz: 0.96 m²/s³ (at 20Hz), other -3dB / octave
Life test of connectors	Board-to-board connector interface can be inserted and removed for 50 times; RF antenna interface cable can be inserted and removed for 30 times.
ESD test	1. Test the power supply PAD and large-area ground in the call status of the module, and the ESD shall meet the following requirements: (1) The contact discharge should pass the test levels of ±4KV and ±5KV (2) Air discharge should pass the test levels of ±8KV and ±10KV 2. When the module is in shutdown status, test the SIM card connector of EVB, and the ESD shall meet the following requirements: (1) The contact discharge should pass the test level of ±4KV (2) Air discharge should pass the test level of ±8KV 3. For other interfaces of the module, ESD shall meet the following requirements: (1) The contact discharge should pass the test level of ±0.5KV (2) Air discharge should pass the test level of ±1KV

6.6 ESD Features

5G SRM815 is a type of consumption terminal product. Although ESD problems have been considered during module design and ESD protection has been completed, considering that there may be ESD problems during transportation and secondary development of 5G SRM815, developers shall consider the protection against ESD problems in the final product. In addition to the anti-static treatment of the package that must be considered, please refer to the recommended circuit for interface design in the document for customer applications.

For the ESD allowable discharge range of 5G SRM815 module, refer to the following table.

Table 41 ESD Performance Parameters (Temperature: 25℃, Humidity: 45%)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Characteristics

This section describes the mechanical dimensions of the module. All dimensions are in mm; for all dimensions without tolerance indicated, the tolerance is ±0.05mm.

7.1 Mechanical Dimensions of the Module

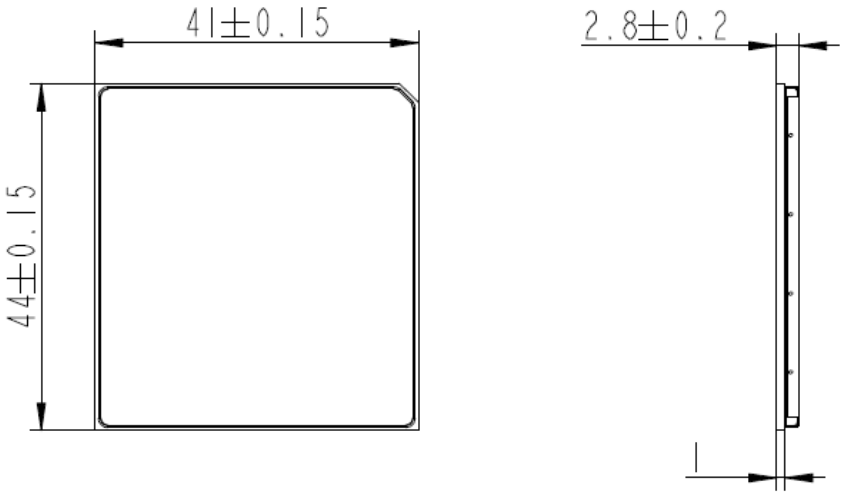

Figure 30 Top and Side Dimensional Drawing (Unit: mm)

7.2 Recommended Packaging

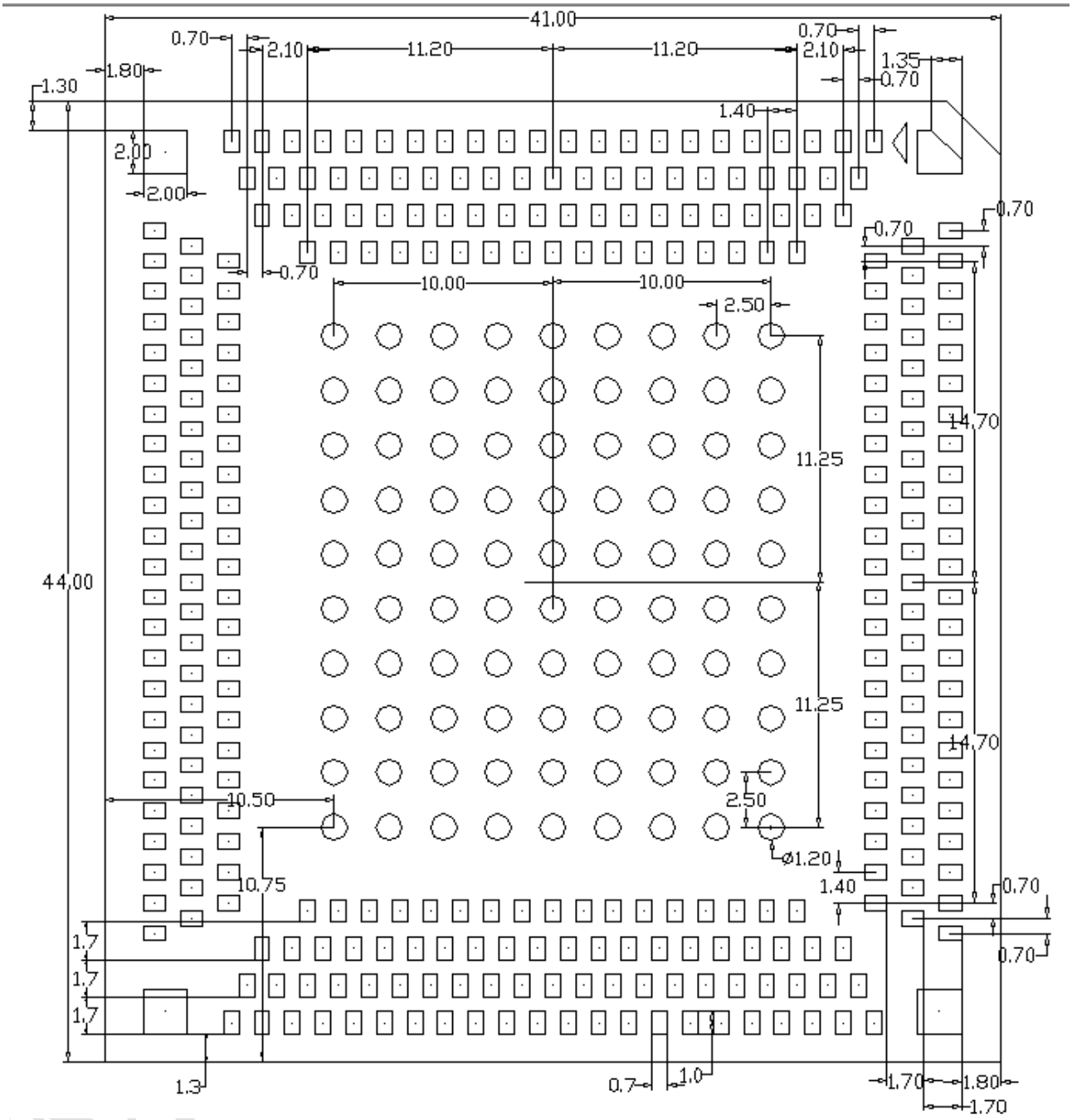

Figure 31 Recommended Packaging (Top View) (Unit: mm)

7.3 Top View of the Module

Figure 32 Top View of the Module

7.4 Bottom View of the Module

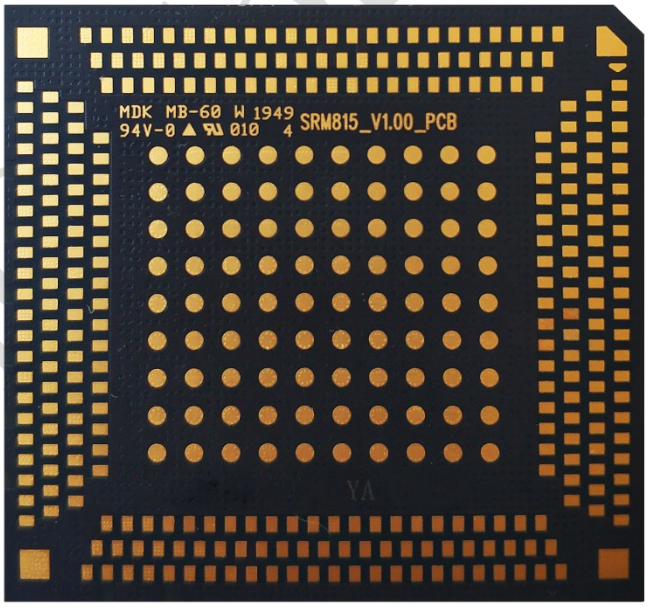

Figure 33 Bottom View of the Module

8 Storage and Production

8.1 Storage

5G SRM815 is delivered in a vacuum-sealed bag. The storage of the module must comply with the following conditions:

1. When the ambient temperature is below 40℃ and the air humidity is lower than 90%, the module can be stored in a vacuum-sealed bag for 12 months;
2. After the vacuum-sealed bag is opened, you can directly conduct solder reflow or other high-temperature processes for the module if the following conditions are met:

- The air humidity for module storage is lower than 10%;
- The ambient temperature of the module is lower than 30℃, the air humidity is lower than 60%, and the factory completes the placement within 72 hours.

3. If the module is in the following conditions, it needs to be baked before placement:

- When the ambient temperature is 23℃ (±5 ℃ fluctuations are allowed), the humidity displayed by the humidity indicator card is greater than 10%;
- After the vacuum-sealed bag is opened, the ambient temperature of the module is lower than 30℃ and the air humidity is lower than 60%, but the factory fails to complete the placement within 168 hours;
- After the vacuum-sealed bag is opened, the air humidity for module storage is greater than 10%.

4. If the module needs to be baked, bake it for 8 hours at 125℃ (±5 ℃ fluctuations are allowed).

Note:
The package of the module cannot withstand such high temperature, please remove the package of the module before the module is baked.

8.2 Production Welding

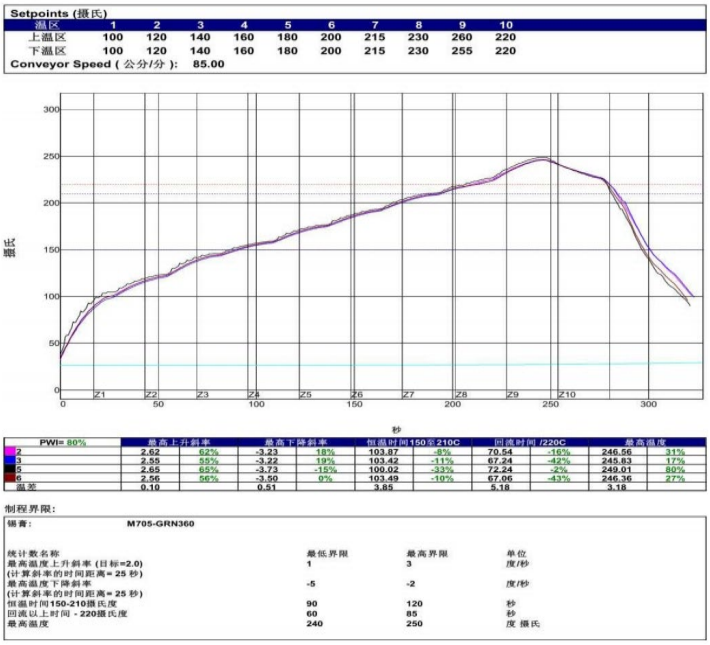

Figure 34 Temperature Curve of Solder Reflow

8.3 Packaging

5G SRM815 will be delivered in vacuum sealed bags.

9 Annex A Reference Documents and Abbreviations

9.1 Reference Documents

- 5G SRM815 module specifications;
- 5G SRM815 AT instruction set;
- 5G SRM815 EVB user manual;
- 5G SRM815 reference design circuit;
- 5G SRM815 application service process manual

9.2 Abbreviations

Table 42 Abbreviations

Abbreviations	Description
AMR	Adaptive Multi-rate
BER	Bit Error Rate
BTS	Base Transceiver Station
PCI	Peripheral Component Interconnect
CS	Circuit Switched (CS) domain
CSD	Circuit Switched Data
DCE	Data communication equipment
DTE	Data terminal equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FR	Frame Relay
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSPA	HSPA High-Speed Packet Access
HSPA+	HSPA High-Speed Packet Access+

IEC	International Electro-technical Commission
IMEI	International Mobile Equipment Identity
MEID	Mobile Equipment Identifier
I/O	Input/Output
ISO	International Standards Organization
ITU	International Telecommunications Union
bps	bits per second
LED	Light Emitting Diode
M2M	Machine to machine
MO	Mobile Originated
MT	Mobile Terminated
NTC	Negative Temperature Coefficient
PC	Personal Computer
PCB	Printed Circuit Board
PCS	Personal Cellular System
PCM	Pulse Code Modulation
PCS	Personal Communication System
PDU	Packet Data Unit
PPP	Point-to-point protocol
PS	Packet Switched
QPSK	Quadrate Phase Shift Keying
SIM	Subscriber Identity Module
TCP/IP	Transmission Control Protocol/ Internet Protocol
UART	Universal asynchronous receiver-transmitter
USIM	Universal Subscriber Identity Module
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WCDMA	Wideband Code Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TDD-LTE	Time Division Long Term Evolution
FDD-LTE	Frequency Division Duplexing Long Term Evolution
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value

10. Annex B GPRS Coding Scheme

Table 43 Description of Different Coding Schemes

Mode	CS-1	CS-2	CS-3	CS-4
Code rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data rate Kb/s	9.05	13.4	15.6	21.4